# Dust Networks

## Eterna LTP5901 / LTP5902 Integration Guide

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# Design Process

The design process when working with the LTP590x module based products varies based upon the products use. For customers not using the OCSDK in SmartMesh IP motes, SmartMesh WirelessHART motes and SmartMesh IP Managers the LTP590x based products should be treated like fixed function ICs programmable ICs. Connect to the devices IOs as described in the respective data sheet and include a programming header / test points to provide a method to load software onto the product. Products are **not** shipped with software preloaded.

For customers writing applications on the OCSDK the LTP590x products should be treated much like a microcontroller product with a few key exceptions. The integration guide focuses on the steps to design and manufacture LTP590x module based PCAs. Design of a system solution should be completed with an understanding of the integration guide and the network as described in either the SmartMesh IP User Guide or the SmartMesh WirelessHART User Guide. In addition, if developing software on the LTP590x-IPM, the software development process and API definitions are provided on www.dustcloud.org.

After defining how the product(s) should operate in network and how the design will be partitioned between hardware and software the design will typically take the following steps:

1) Review the example schematic provided in this document to gain familiarity with the required additional PCA components.
2) For customers developing software on the LTC5901/2-IPM, use the Fuse Table application as described in the Eterna Board Specific Configuration Guide to assign functions, such as SPI, I2C and GPIO to IOs. Start by loading the default Fuse Table for the LTP50x product. Fuse Tables can be found in the SmartMesh IP.zip file on a customer account at https://www.linear.com/mylinear/login.php
3) Follow this document to complete the schematic design and layout.
4) Use the Fuse Table application as described in the Eterna Board Specific Configuration Guide to create a fuse table for the design.
5) Use the Eterna Serial Programmer to load all of the required images onto the LTP590x, the Fuse Table, Loader, Partition table and Image.
6) Develop and debug the design.
7) Develop production tests. The Eterna Serial Programmer is intended for loading flash images in production. The LTC5800 BDSL file provides an efficient method to test PCB interconnect.
8) The ETERNA2 Users Guide provides guidelines for antenna usage and regulatory documentation requirements for the geographies the LTP590x products have been certified. In addition, the guide includes a complete set of the LTC5800 specific information and commands required to certify an LPT590x based PCB worldwide. Certification can be a lengthy process requiring significant supporting documentation from the manufacturer. Customers are recommended to work with a certification agency familiar with the regulations in the geography/geographies the design will be certified.

# About This Guide

This document provides the design guidelines essential for incorporating either an Eterna LTP5901 or LTP5902 module. The document covers design, layout, EMI, and some manufacturing considerations.

## Audience

This document is intended for system developers, hardware designers, and layout engineers.

## Related Documents

The following related documents are available:

Eterna Serial Programmer Guide
ETERNA2 User's Guide
Eterna Board Specific Configuration Guide

## Conventions and Terminology

This guide uses the following text conventions:

- `Computer type` indicates information that you enter, such as a URL.
- **Bold type** indicates buttons, fields, and menu commands.
- *Italic type* is used to introduce a new term.
- **Note:** Notes provide more detailed information about concepts.
- **Caution:** Cautions advise about actions that might result in loss of data.
- **Warning:** Warnings advise about actions that might cause physical harm to the hardware or your person.

## Revision History

| Revision | Date | Description |
|---|---|---|
| **040-0119 rev 1** | 6/7/2012 | Initial version |
| **040-0119 rev 2** | 7/18/2012 | Updated references |
| **040-0119 rev 3** | 8/20/2012 | Corrected keep out for LTP5901 land pattern |
| **040-0119 rev 4** | 4/2/2013 | Added support documentation for external SRAM. |
| **040-0119 rev 5** | 5/8/2013 | Added hyper link to programmer. |
| **040-0119 rev 6** | 10/24/2013 | Update SDRAM schematics and BOM |
| **040-0119 rev 7** | 1/16/2014 | Added description for LTP5902 mechanical leads |
| **040-0119 rev 8** | 1/11/2016 | Added Design Process Section<br>Added description of Software Version / Part Number dependency. |

# 1 Design Guidelines

## Schematic Design

The LTP5901 and LTP5902 require little external circuitry, as the devices references, decoupling and power supply filtering are integrated. The LTP5901 and LTP5902 have been modularly certified for operation in many geographies – see the ETERNA2 User's Guide for the currently supported geographies and regulatory related specifications. If further certifications may be necessary, it is essential to provide a method to deliver specific radio test APIs via the API UART interface during testing. Test connections should be included in the schematic if the product does not provide a natural means of delivering the API calls.

**LTP5901 and LTP5902 are not shipped with software pre-loaded**. Customers are required to load software onto the LTP5901 / LTP5902 during development and production. The Eterna Serial Programmer can be used to load all of the required images onto the LTP590x, the Fuse Table, Loader, Partition table and Image. Refer to the software release zip file available from https://www.linear.com/mylinear/login.php for software images and programming instructions.

The schematic shown in Figure 1 includes the signal connections necessary for the programming header. The part number for the header is provided in Table 1.

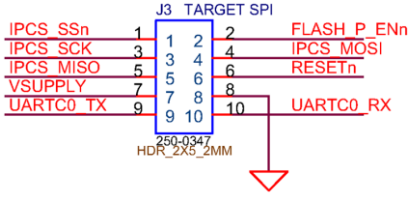


**Figure 1 Eterna Example Schematic**

**Table 1 Programming Header**

| Reference | Value | Vendor | Vendor P/N |
|---|---|---|---|
| J3 | 5x2 header | Molex | 87831-1020 |

### Manager Variations –IPMA –IPRA, -IPRB, -IPRC

Manager hardware dependencies were changed with the release of SmartMesh IP Manager software release 1.2.4. Releases earlier than 1.2.4 require the use of specific matching hardware to versions which supported the use of external memory. For customers using release 1.2.3 or prior see the following subsection: Manager Variations –IPRA, -IPRB, -IPRC. When using SmartMesh IP Manager software release 1.2.4 and later see the following subsection: Manager Variations –IPMA (Only for Software versions 1.2.4 and later)

***Manager Variations –IPMA (Only for Software versions 1.2.4 and later)***

Without the addition of external SRAM, Eterna IP managers are limited to supporting networks of 32 or fewer motes. Eternal memory may be added to Eterna IP Manager products to:

a. manage networks of up to 100 motes and,

b. increase throughput of the manager from 24 to 36 packets per second

To support external RAM with software release 1.2.4 or later customers must either create a Fuse Table image or install a Fuse Table image configured for external memory support. See the Eterna Board Specific Configuration Guide for instructions on how to create a fuse table image. See the file, Readme - File Organization and Programming Instructions.pdf, in the Eterna subdirectory of the SmartMesh IP zip file available from https://www.linear.com/mylinear/login.php to locate the default fuse table image. To support external SRAM customers should use the fuse table corresponding to the product (either LTP5901 or LTP5902) which includes the "–IPRB" sub-string in the file name. To support a design **without** external SRAM customers should use the fuse table corresponding to the product (either LTP5901 or LTP5902) which includes the "–IPRA" sub-string in the file name.

The schematic shown in Figure 2 and Figure 3 includes all the external connections and components necessary to add the external RAM. The connections differ from the configuration without external RAM as follows:

1) CLI access is on UARTC1, not UARTC0

2) Mapping of external bus signals to Eterna's general purpose function pins

3) The Memory, latches and pulse generators shown in Figure 3

The reference Bill of Materials (BOM) for the addition components needed for the external memory interface is shown in Table 2.

***Manager Variations –IPRA, -IPRB, -IPRC (Only for Software versions 1.2.3 and earlier)***

Without the addition of external SRAM, Eterna IP managers are limited to supporting networks of 32 or fewer motes. Eternal memory may be added to Eterna IP Manager products to:

c. manage networks of up to 100 motes – and / or –

d. increase throughput of the manager from 24 to 36 packets per second

The LTP5901/LTP5902-IPRA is limited to supporting a maximum of 32 motes and a maximum throughput of 24 packets per second. The LTP5901/LTP5902-IPRA does not support the use of external RAM.

The LTP5901/LTP5902-IPRC natively supports up to 32 motes with a maximum throughput of 36 packets per second. A license key can be purchased to raise the limit of the LTP5901/LTP5902-IPRC maximum network size to 100 motes. Contact your Linear Sales representative for details on how to order license key certificates. The certificate contains a product key and instructions for requesting the generation of a license key, which typically takes one to two business days to receive a license key. License keys are entered via either the **set config** command documented in SmartMesh IP Manager CLI Guide or the **setLicense** command documented in the SmartMesh IP Manager API Guide. The LTP5901/LTP5902-IPRC requires the use of external RAM.

The LTC5800-IPRB supports networks of up to 100 motes and has a maximum throughput of 36 packets per second The LTP5901/LTP5902-IPRB requires the use of external RAM.

The schematic shown in Figure 2 and Figure 3 includes all the external connections and components necessary to add the external RAM. The connections differ from the LTP5901-IPRA as follows:

4) CLI access is on UARTC1, not UARTC0

5) Mapping of external bus signals to Eterna's general purpose function pins

6) The Memory, latches and pulse generators shown in Figure 3

The reference Bill of Materials (BOM) for the addition components needed for the external memory interface is shown in Table 2.

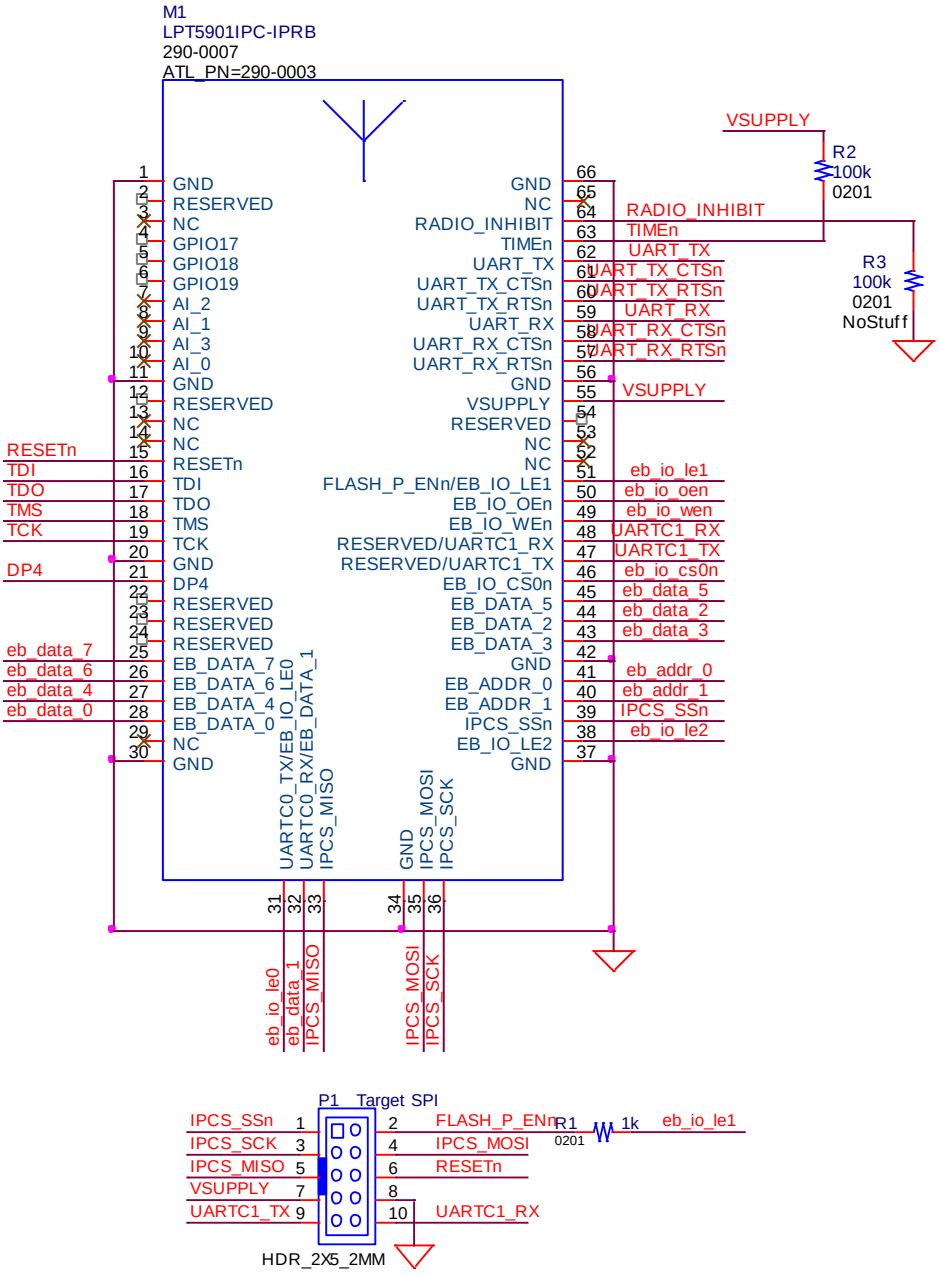


**Figure 2 Eterna Extended Memory Example Schematic (page 1 of 2)**

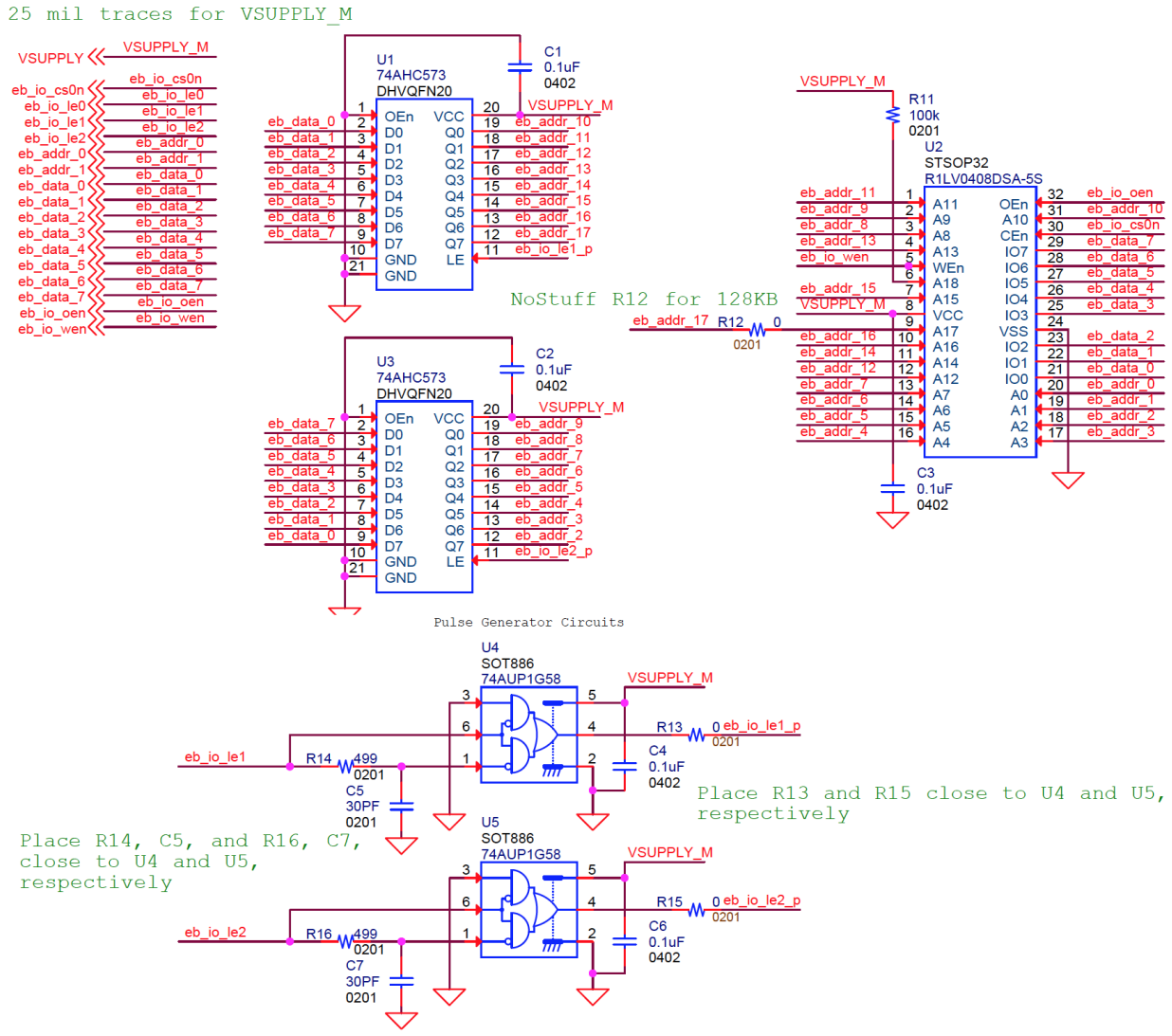


**Figure 3 Eterna Extended Memory Example Schematic (page 2 of 2)**

Eterna's External memory function has been tested with the BOM options shown in Table 2. The RAM components shown have been selected for low power operation and their use will result in an increase of a few µA of current consumption. For designs that are not energy constrained, substitution of general purpose RAMs with equal or faster speed grades should be possible. Substitution of the multi-function logic and octal latch components should be done carefully to maintain the timing generated by the pulse generation circuits.

**Table 2 External Memory Reference Bill of Materials**

| Reference | Value | Vendor | Vendor P/N |
|---|---|---|---|
| R12, R13, R15 | 0 | Panasonic | ERJ-1GE0R00C |
| R2, R3, R11 | 100 kOhm | Panasonic | ERJ-1GEJ104C |
| R14, R16 | 499 Ohm | Vishay | CRCW0201499RFKED |
| R1 | 1 kOhm | Panasonic | ERJ-1GEJ102C |
| R10 | 237 Ohm | Vishay | CRCW0402237RFKED |
| C5, C7 | 30 pF | Murata | GRM0335C1E300JD01D |
| C1, C2, C3, C4, C6 | 100 nF | Murata | GRM155R71C104KA88D |
| U2 | 128K x 8-bit RAM | Cypress | CY62128EV30LL-45ZAXI |
| U2 Alternate | 128K x 8-bit RAM | Renesas | R1LV0108ESA-5SI#B0 |
| U4, U5 | Multifunction Logic | NXP | 74AUP1G58GM, 132 |
| U1, U3 | Octal Latch | NXP | 74AHC573BQ,115 |
| P1 | 5x2 header | Molex | 87831-1020 |
| M1 | ETERNA Module (chip antenna) | Linear | LTP5901IPC-IPMA |
| M1 (alt. application) | ETERNA Module (MMCX connector) | Linear Technology | LTP5902IPC-IPMA |
| M1 (alt. application) | ETERNA Module (32-mote network, chip antenna) | Linear Technology | LTP5901IPC-IPRC |
| M1 (alt. application) | ETERNA Module (100-mote network, chip antenna) | Linear Technology | LTP5901IPC-IPRB |
| M1 (alt. application) | ETERNA Module (32-mote network, MMCX connector) | Linear Technology | LTP5902IPC-IPRC |
| M1 (alt. application) | ETERNA Module (100-mote network, MMCX connector) | Linear Technology | LTP5902IPC-IPRB |

## PCB Layout

Eterna-based designs should adhere to the following layout-sensitive guidelines:

1. The Eterna modules include exposed test points, and pads on the bottom (mounting) side of the PCB. Exposed metal should be avoided in the on the top surface of the mating PCB in the area where the module will be mounted.
2. The LTP5901 includes a chip antenna with layout designed to work over 1 mm thick FR4, as used in the LTP5902. It is recommended to maintain an opening free of FR4 and any conductive material as far as practically possible to maximize the radio performance.

3. The LTP5902 includes a through hole mounted MMCX connector. A sufficient opening in the mating PCB must be provided – see the LTP5902 recommended land pattern later in this document for details.
4. Eterna's radios can be sensitive to EMI generated by DC/DC converters. It is recommended that such inductors are placed a minimum of 2 inches from the radio and antenna or MMCX connector. If space constraints prevent this degree of separation, inductor selection can reduce the EMI generated. Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but generally cost more than powdered iron core inductors with similar electrical characteristics.

## Eterna LTP5901 Recommended Land Pattern (Chip Antenna)

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5901 and tolerances for metal etch are commonly more precise than solder mask deposition, the recommended practice is to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

Land Pattern dimensions are illustrated in Figure 4.

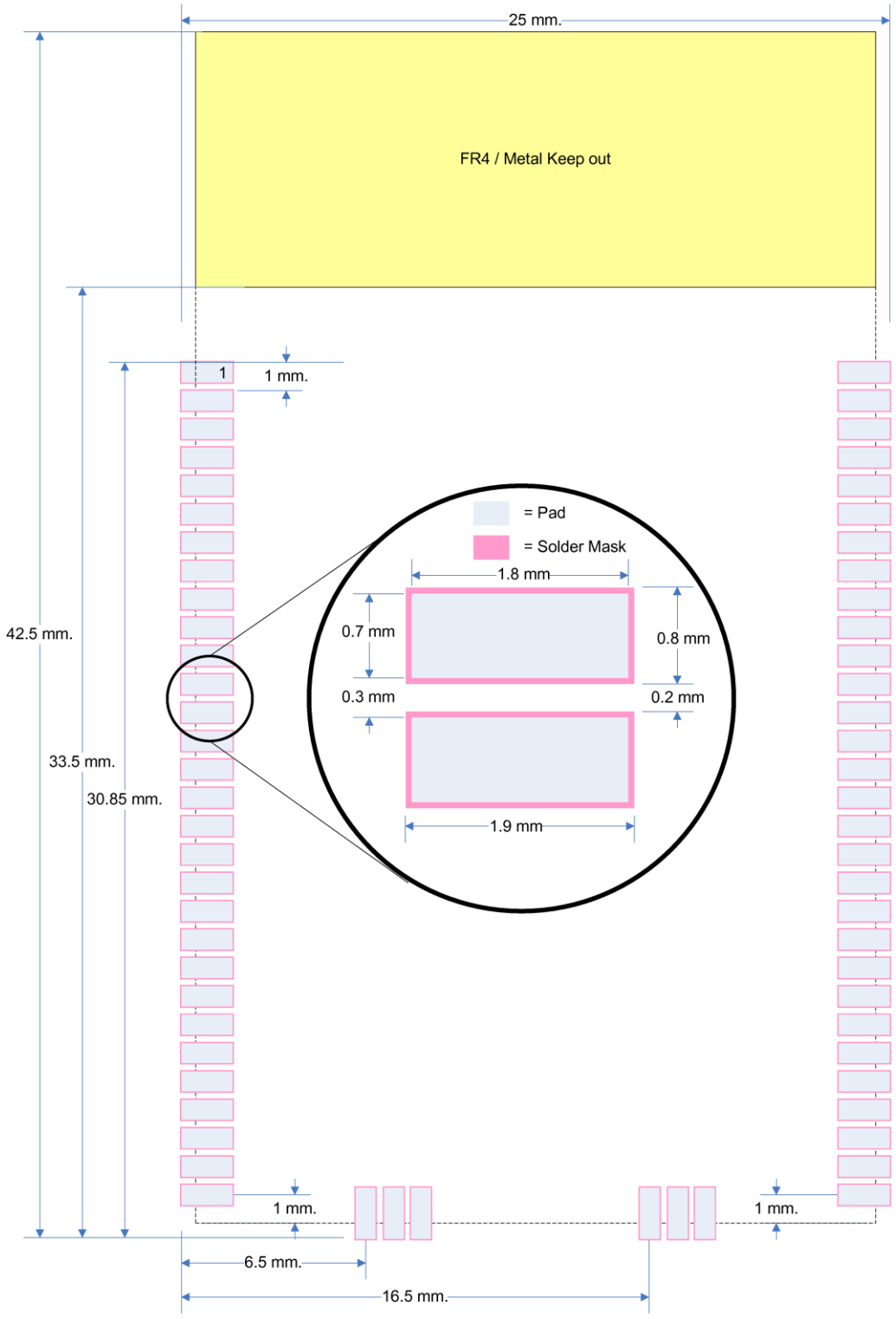


**Figure 4 LTP5901 Land Pattern (Chip Antenna)**

## Eterna LTP5902 Recommended Land Pattern (MMCX)

Two common practices for defining land patterns are Non Solder Mask Defined, NSMD, and Solder Mask Defined, SMD. Given the lead pitch of the LTP5902 and tolerances for metal etch are commonly more precise than solder mask deposition, the recommended practice is to use NSMD land patterns. The solder mask opening should provide sufficient margin for registration tolerance to avoid solder mask infringing on the pad, typically 60 to 75 um from the edge of the pad and the solder mask.

The LTP5902 includes 4 mechanical leads, the corresponding pads labeled M in in Figure 5, are recommended to be soldered to the carrier PCB for designs targeting high vibration applications. Recommended practice is not to connect mechanical leads to ground or any other signal on the carrier PCB.

Land Pattern dimensions are illustrated in Figure 5.

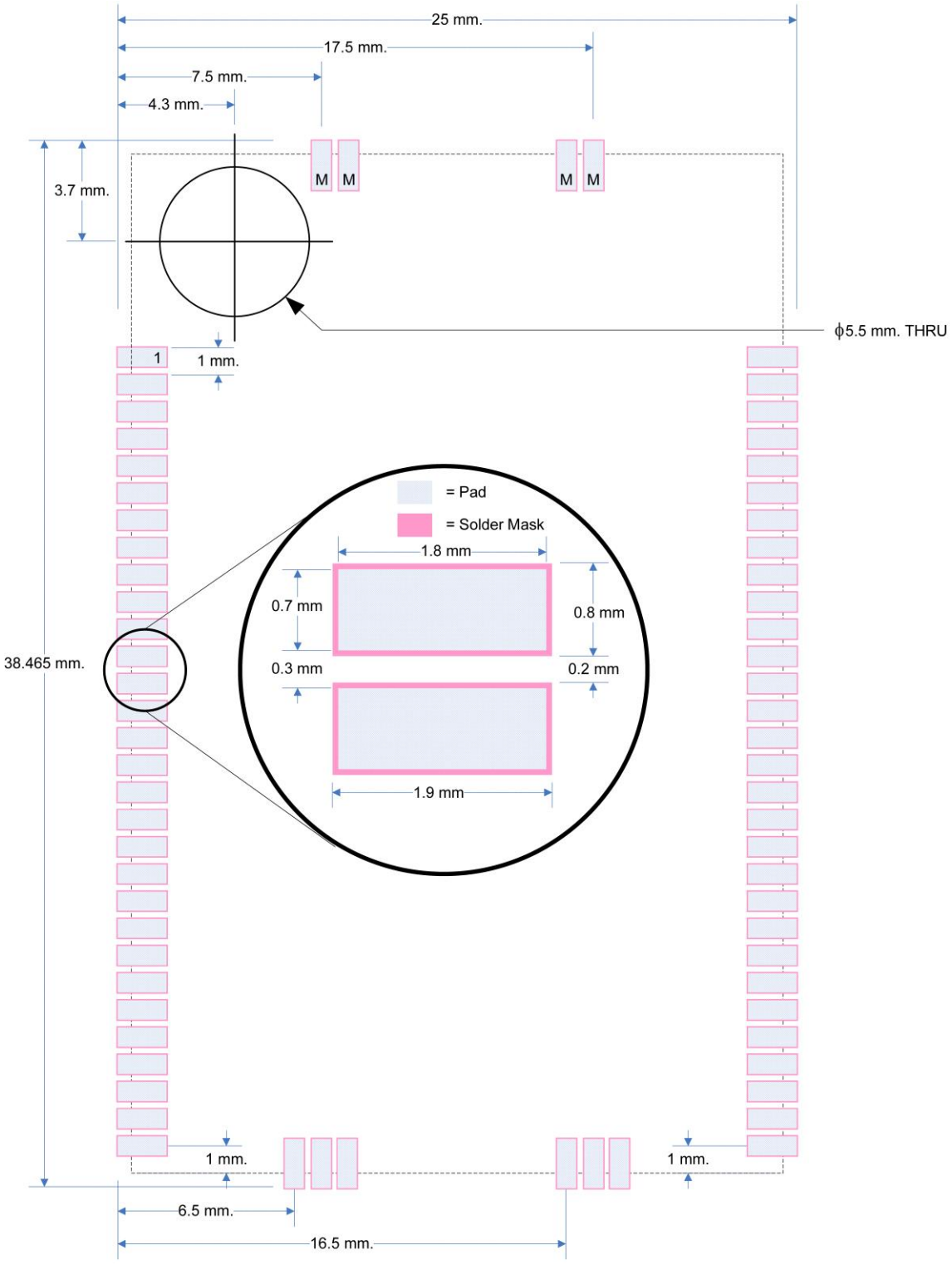


**Figure 5 LTP5902 Land Pattern (MMCX)**

## Antenna ESD Considerations

The antenna pin is a particularly sensitive node for electro-static discharge (ESD) since it must detect small, high-frequency signals. ESD damage may result in decreased receive or transmit performance, or other system failure. Many applications for Eterna have an exposed antenna that provides an entry point for ESD events. Proper consideration of antenna design as well as antenna protection can substantially improve ESD robustness in harsh environments.

A radome (protective covering) made of highly resistive material may be used to prevent direct contact with the antenna and/or dissipate charge. To avoid ESD events caused by triboelectric charging generated by wind passing over the antenna in dry climates, the radome design should consider bulk and surface resistivity as well as the size of the gap between the antenna metal and the interior of the radome.

In general, DC-grounded antennas (the antenna and ground have a DC short) provide superior protection to ESD events. DC-grounded antennas are highly recommended in harsh environments. Additionally, a DC path-to-earth ground should be provided whenever possible to help bleed off accumulated charge from the antenna as well as leak charge from the radome.

While these general guidelines should improve robustness to ESD events, individual implementations may have unique factors that complicate ESD protection.

## Supply Design

Due to the heavy duty cycling, Eterna's current consumption can change substantially over a short period. This does not represent an issue for systems with supplies having low source impedance (less than 5 Ohms). Regulated supplies, however, may have difficulty in the sudden changes in current consumption (more than an order of magnitude in less than 1 µs), resulting in transient voltages on the supply co-incident with the higher current consumption of the radio operation. To ensure proper operation of the radio, a supply should be able to ramp from 250 µA to 10 mA in less than 1 µs without generating a transient greater than 200 mV. For systems with regulated supplies, consultation with Linear Technology is strongly recommended.

Eterna can be configured to support current limited supplies. Contact Linear Technology for details.

## Voltage Supervision and Reset

Eterna includes a power-on reset to safely set its own state during power up, and includes a brown-out circuit that immediately halts flash erase cycles and interrupts flash write cycles at the next 32-bit boundary, generating an interrupt to the CPU and maintaining state for the CPU to correct should the power supply return to normal operating levels. In the interest of avoiding flash corruption, it is **not** considered best practice to connect the RESETn lead to a voltage supervisor or to asynchronously assert RESETn without previously suspending network and flash activity.

# 2 Manufacturing Guidelines

## Reflow

Given that Eterna modules are assembled using either “SAC305”, "Alpha OM-338 CSP" or " SMIC ECO M705-GRN360" No Clean Solder Paste, careful adherence to J-STD-020 to avoid reflowing the modules during the assembly process is necessary. The solder joint quality of the “castellations” where they contact the mating PCB should meet IPC-A-610 Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations.

## Solder Paste/Cleaning

“No Clean” soldering paste is strongly recommended, as it does not require cleaning following the soldering process. Cleaning the populated modules is strongly discouraged due to the potential issues that may result. Residuals under the module are difficult to remove with any cleaning process. Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module, potentially resulting in combination with soldering flux residuals leading to short circuits between neighboring pads. Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals under the shield, which is not accessible for post-washing inspection. Ultrasonic cleaning could damage the module permanently.

## Packaging

The LTP5901 and LTP5902 modules are MSL3, however baking is required when parts are packaged in individual ESD bags.

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