

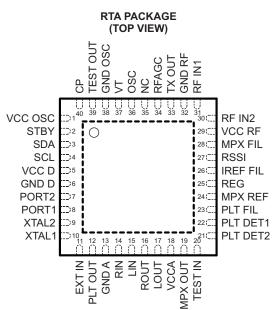
FEATURES

- Single-Chip FM Stereo Radio and Transmitter
- FM Stereo MPX [Receive (Rx), Transmit (Tx)]
- Frequency Range 76 MHz to 108 MHz (Rx, Tx)
- Low Supply Current
 - Rx: 11.5 mA (V_{CC} = 3 V, No RF Input)
 - Tx: 13 mA (V_{CC} = 3 V, No Audio Input, RTX = Open)
- 32.768-kHz Crystal
- I²C Interface
- MPX Output for RDS (Rx)
- Seek Tuning (Rx)
- RFAGC (Rx)
- RF Auto-Power Control (Tx)
- Pilot Cancel (Rx)
- Sixth-Order 15-kHz LPF (Tx)
- Programmable De/Pre-Emphasis (50/75 μs)

- Pilot Out (Tx)
- General-Purpose External Input (Tx)
- High Power Selectable RF Output (Tx) -7/-3/1/4 dBm
- High Cut Control (HCC), Stereo Noise Control (SNC) (Rx)
- Soft Mute (Rx)
- $V_{CC} = 2.5 \text{ V to } 4 \text{ V}$
- 40-Pin QFN Package

APPLICATIONS

- Portable Media Players
- MP3 Players
- Personal Navigation Devices



NC - No internal connection

DESCRIPTION

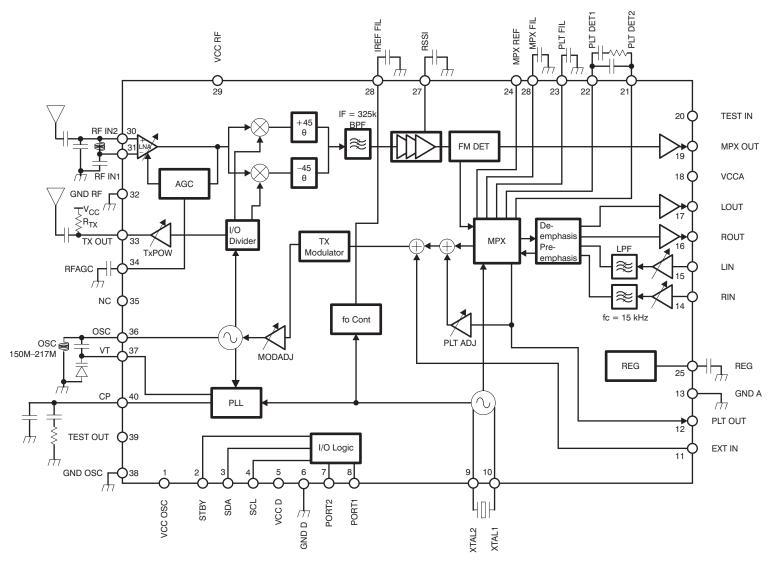
The SN761633 is an FM radio receiver and transmitter IC for portable audio players.

The circuit consists of a stereo FM radio receiver and FM transmitter, and is available in a small-outline package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



TEXAS INSTRUMENTS www.ti.com

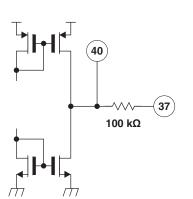
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TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	COLIEMATIC
NAME NO.		DESCRIPTION	SCHEMATIC
СР	40	Charge-pump output	Figure 1
EXT IN	11	External signal input	Figure 2
GND A	13	Analog ground	
GND D	6	Digital ground	
GND OSC	38	Oscillator ground	
GND RF	32	RF ground	
IREF FIL	26	Reference current filter	Figure 3
LIN	15	Audio left input	Figure 4
LOUT	17	Audio left output	Figure 5
MPX FIL	28	MPX PLL filter	Figure 6
MPX REF	24	MPX reference voltage filter	Figure 7
MPX OUT	19	MPX output	Figure 8
NC	35	Not connected	
OSC	36	Oscillator input	Figure 9
PLT DET1, PLT DET2	22, 21	Pilot detector PLL loop filter	Figure 10
PLT FIL	23	Pilot level detector filter	Figure 11
PLT OUT	12	Pilot signal output	Figure 12
PORT1, PORT2	8, 7	Port output	Figure 13
REG	25	Regulator filter	Figure 14
RF AGC	34	RFAGC filter	Figure 15
RF IN1, RF IN2	31, 30	RF input	Figure 16
RIN	14	Audio right input	Figure 4
ROUT	16	Audio right output	Figure 5
RSSI	27	RSSI filter	Figure 17
SCL	4	I ² C clock input	Figure 18
SDA	3	I ² C data input/output	Figure 19
STBY	2	Standby control input	Figure 20
TEST IN	20	Test input	Figure 21
TEST OUT	39	Test output	Figure 22
Tx OUT	33	Transmitter output	Figure 23
VCC A	18	Analog power supply	
VCC D	5	Digital power supply	
VCC OSC	1	Oscillator power supply	
VCC RF	29	RF power supply	
VT	37	Tuning voltage output	Figure 1
XTAL1, XTAL2	10, 9	Crystal oscillator input/output	Figure 24

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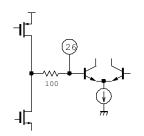
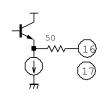


Figure 3. IREF FIL



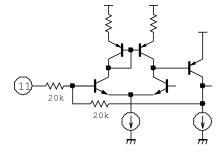


Figure 2. EXT IN

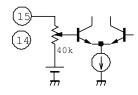


Figure 4. LIN and RIN

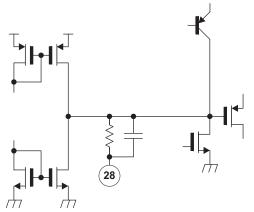
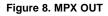


Figure 6. MPX FIL







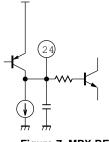


Figure 7. MPX REF

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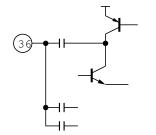
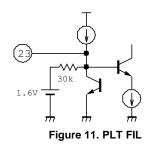


Figure 9. OSC



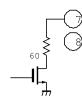
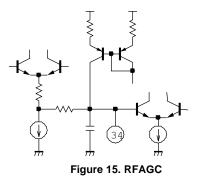


Figure 13. PORT1 and PORT2



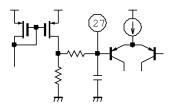


Figure 17. RSSI

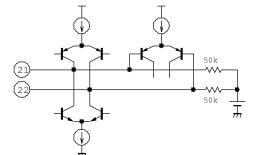


Figure 10. PLT DET1 and PLT DET2



Figure 12. PLT OUT

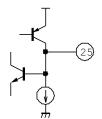


Figure 14. REG

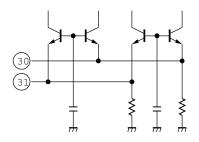
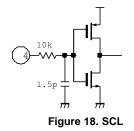
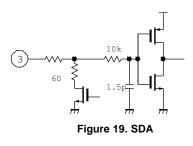


Figure 16. RFIN1 and RFIN2



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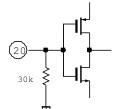
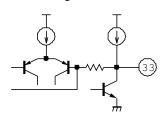


Figure 21. TEST IN

Figure 23. Tx OUT



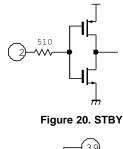


Figure 22. TEST OUT

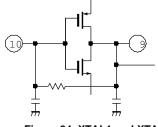


Figure 24. XTAL1 and XTAL2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	I MAX	UNIT
V_{CC}	Supply voltage range	VCCA, VCCD, VCC RF	-0.3	60	V
V _{IN}	Input voltage range	Other pins	-0.3	V _{CC}	V
T _A	T _A Operating free-air temperature range		-20) 85	°C
T _{stg}	Storage temperature range		-65	5 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	VCCA, VCCD, VCC RF, VCC OSC	2.5	3	4	V
T _A	Operating free-air temperature		-20		85	°C

CAUTION:

The SN761633 has four V_{CC} pins (VCCA, VCCD, VCC OSC, and VCC RF). Use of a single power source for all V_{CC} pins is recommended. In the case of multiple power supplies, VCCD should be applied first.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ELECTRICAL CHARACTERISTICS – TOTAL DEVICE

 $V_{CC} = 3 \text{ V}, \text{ T} = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF input voltage (V_{RF}) = 60 dBµVemf; RF frequency (f_{RF}) = 98.1 MHz, Audio signal frequency (f_{AF}) = 1 kHz, Mono, FM = 22.5 kHzdev (30% at 75-kdev Ref.), BW = LPF 30k (unless otherwise noted)

Supply Voltages and Currents

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
V _{CC}	Supply voltage	VCCA, VCCD, VCC RF, and VCC OSC are the same voltage	2.5	3	4	V
I _{CC Rx}	Rx-mode supply current	No RF signal input		11.5		mA
I _{CC Tx1}	Tx-mode supply current 1	No LIN/RIN input, TxPOW[1:0] = 00, R _{Tx} = open		13		mA
I _{CC Tx2}	Tx-mode supply current 2	No LIN/RIN input, TxPOW[1:0] = 00, R _{Tx} = open, DIS_AFLPF = 1		12		mA
I _{CC Tx3}	Tx-mode supply current 3	External input only mode, EN_EXTIN = 1, DIS_LRIN = 1, DIS_AFLPF = 1, TxPOW[1:0] = 00, R_{Tx} = open		11.5		mA
I _{CC Tx4}	Tx-mode supply current 4	No LIN/RIN input, TxPOW[1:0] = 10, R_{Tx} = 300 Ω		18		mA
I _{CC Tx5}	Tx-mode supply current 5	No LIN/RIN input, TxPOW[1:0] = 11, R_{Tx} = 150 Ω		24		mA
I _{CC STBY1}	Standby supply current 1	STBY (bit) = 1		0.1	10	μA
I _{CC STBY2}	Standby supply current 2	STBY (2 pin) = GND		0.1	10	μA

Crystal Oscillator

PARAMETER		TEST CONDITIONS	TYP	UNIT
f_{XTAL}	Crystal oscillator frequency	Crystal $C_L = 12.5 \text{ pF}$	32.768	kHz

Voltage-Controlled Oscillator

PARAMETER		MIN	MAX	UNIT
f _{OSC}	f _{OSC} Oscillator frequency range		217	MHz

Synthesizer

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Ν	Programmable counter	14 bit			16383	
f _{REF}	Reference frequency for phase detector			16.384		kHz
f _{STEP}	Tuning frequency step			8.192		kHz
f _{RANGE} US			10707		13237	dec
	US/EU band range for search stop	$LOC_HL = 1$	87.387	1	08.113	MHz
		LOC_HL = 0	10628		13157	dec
			87.390	1	08.107	MHz
	Japan band range for search stop	LOC_HL = 1	9304		11039	dec
4			75.893		90.107	MHz
f _{RANGE} JPN			9224		10960	dec
		$LOC_HL = 0$	75.888		90.109	MHz
		CP[1:0] = 00		0.6		
		CP[1:0] = 01		1.25		•
I _{CP}	Charge-pump current	CP[1:0] = 10		2.5		μA
		CP[1:0] = 11		5		

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I²C Interface

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V _{IH}	High-level input voltage (SCL, SDA)		$0.7 imes V_{CC}$		V
VIL	Low-level input voltage (SCL, SDA)			$0.3 \times V_{CC}$	V
V _{OL}	Low-level ouput voltage (SDA)	V_{CC} = 3 V, I_{OL} = 500 μ A		0.4	V
f _{SCL}	Clock frequency (SCL)			400	kHz

ELECTRICAL CHARACTERISTICS – Rx BLOCK

 $V_{CC} = 3 \text{ V}, T_A = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF input voltage (V_{RF}) = 60 dBµVemf, RF frequency (f_{RF}) = 98.1 MHz, Audio signal frequency (f_{AF}) = 1kHz, Mono, FM = 22.5 kHzdev (30% at 75-kdev Ref.), BW = LPF 30 k (unless otherwise noted)

RF Signal Input

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{TU RANGE}	Tuning frequency range		76		108	MHz
V _{Rx}	Sensitivity input voltage	$(S+N)/N = 26 \text{ dB}, 22.5\text{-kHz dev}, \text{De-emphasis} = 75 \ \mu\text{s}$		10		dBµVemf
R _{RFIN}	Input resistance	RF IN at 100 MHz, No RF signal input		120		Ω
C _{RFIN}	Input capacitance	RF IN at 100 MHz, No RF signal input		1.5		pF
IR _{Rx}	Image rejection ratio			30		dB

IF Band-Pass Filter

PARAMETER		TEST CONDITIONS	TYP	UNIT
f _{IF}	IF center frequency	Peak frequency, Test mode	325	kHz
B _{IF}	IF bandwidth	–3 dB, Test mode	130	kHz
S ₊₂₀₀	Selectivity high side (200 kHz)	325 kHz + 200 kHz, Test mode	25	dB
S_200	Selectivity low side (200 kHz)	325 kHz – 200 kHz, Test mode	30	dB
S ₊₁₀₀	Selectivity high side (100 kHz)	325 kHz + 100 kHz, Test mode	8	dB
S_100	Selectivity low side (100 kHz)	325 kHz – 100 kHz, Test mode	7	dB

FM Demodulator MPX OUT

	PARAMETER	TEST CONDITIONS	TYP	UNIT
V _{MPXOUT}	MPX OUT output level	22.5 kHz dev, f _{AF} = 1 kHz, EN_MPXOUT = 1	75	mVrms

Soft Mute

PARAMETER		TEST CONDITIONS		UNIT
V _{S MUTE}	Soft mute start point	S_MUTE = 1, -3 dB	11	dBµVemf
ATT _{S MUTE}	Soft mute attenuation	V_{RF} = 60 dBµVemf, S_MUTE = 0 to 1, 0 V applied to RSSI pin externally as pseudo condition of no RF signal input	18	dB

ELECTRICAL CHARACTERISTICS – Rx BLOCK (CONTINUED)

 $V_{CC} = 3 \text{ V}, T_A = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF input voltage (V_{RF}) = 60 dBµVemf, RF frequency (f_{RF}) = 98.1 MHz, audio signal frequency (f_{AF}) = 1kHz, Mono, FM = 22.5 kHzdev (30% at 75 kdev Ref.), BW = LPF 30 k (unless otherwise noted)

High Cut Control

	PARAMETER	TEST CONDITIONS		TYP	UNIT	
TC _{DE EM} De-empha	De-emphasis time constant	$V_{\rm e} = 60 \mathrm{dPu} \mathrm{(omf)}$	EMTC = 0	50		
	De-emphasis time constant	$V_{RF} = 60 \text{ dB}\mu\text{Vemf},$	EMTC = 1	75	μs	
		$V_{RF} = 60 \text{ dB}\mu\text{Vemf},$	EMTC = 0	150		
TC _{DE EM HCC}	De-emphasis time constant on HCC applied	V _{RF} = 60 dBµVemf, 0 V applied to RSSI pin externally as pseudo condition of no RF signal input	EMTC = 1	225	μs	

MPX Decoder

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{O MONO}	Mono output level	Mono, 22.5 kHzdev, f _{AF} =1 kHz, De-emphasis = 75 μs		75		mVrms
V _{O ST}	Stereo output level	L = R, 22.5 kHzdev, f_{AF} =1 kHz, De-emphasis = 75 μ s, Pilot = 7.5 kHzdev (10%)		75		mVrms
V _{DIFF}	LOUT- and ROUT-level difference	L = R, 22.5 kHzdev, f_{AF} = 1 kHz, De-emphasis = 75 μ s, Pilot = 7.5 kHzdev (10%) LOUT-level ref.	-1		1	dB
ATT _{MUTE}	MUTE attenuation	MUTE = 1	60			dB
ATT _{L MUTE}	LOUT MUTE attenuation	MUTE_L = 1	60			dB
ATT _{R MUTE}	ROUT MUTE attenuation	MUTE_R = 1	60			dB
f _{ODD}	Overdrive deviation margin frequency	f _{AF} = 1 kHz, De-emphasis = 75 s THD < 3%		150		kHz
S/N _{MONO}	Mono signal-to-noise ratio	75 kHzdev (100%)., f _{AF} = 1 kHz, De-emphasis = 75 μs		60		dB
THD _{MONO}	Mono total harmonic distortion	22.5 kHzdev, f _{AF} = 1 kHz, De-emphasis = 75 μs		0.3		%
S/N _{ST}	Stereo signal-to-noise ratio	67.5 kHzdev (90%)., f _{AF} = 1 kHz, De-emphasis = 75 μs, Pilot = 7.5 kHzdev (10%)		50		dB
THD _{ST}	Stereo total harmonic distortion	22.5 kHzdev, f _{AF} = 1 kHz, De-emphasis = 75 μs, Pilot = 7.5 kHzdev (10%)		1		%
SEP _{ST}	Stereo separation	22.5 kHzdev, f _{AF} = 1 kHz, De-emphasis = 75 μs, Pilot = 7.5 kHzdev (10%)		33		dB
DEV _{PLT DET}	Pilot detect deviation	ST_IND 0 to 1 at I ² C read mode		5		%
HYS _{PLT DET}	Pilot detect deviation hysteresis			2		dB
V _{SWMST}	Mono-to-stereo switch level	22.5 kHzdev, f_{AF} = 1 kHz, De-emphasis = 75 µs, Pilot = 7.5 kHzdev (10%), SNC = 0		33		dBµVemf
HYS _{SWMST}	Mono-to-stereo switch-level hysteresis	22.5 kHzdev, f _{AF} = 1 kHz, De-emphasis = 75 μs, Pilot = 7.5 kHzdev (10%), SNC = 0		2		dB

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ELECTRICAL CHARACTERISTICS – Rx BLOCK (CONTINUED)

 $V_{CC} = 3 \text{ V}, T_A = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF input voltage (V_{RF}) = 60 dBµVemf, RF frequency (f_{RF}) = 98.1 MHz, Audio signal frequency (f_{AF}) = 1kHz, Mono, FM = 22.5 kHzdev (30% at 75-kdev ref.), BW = LPF 30 k (unless otherwise noted)

Stereo Noise Control

	PARAMETER	TEST CONDITIONS	TYP	UNIT
V _{SNC}	SNC start point	22.5 kHzdev, $f_{AF} = 1$ kHz, Pilot = 7.5 kHzdev (10%), SNC = 1, Separation = 20 dB	36	dBµVemf

RSSI

	PARAMETER	TEST CONDITIONS	ТҮР	UNIT
V _{RSSI MIN}	RSSI minimum input level	RSSI[3:0] 0 to1 (dec) at I ² C read mode	9	dBµVemf
RES _{RSSI}	RSSI resolution		2	dB

IF Counter

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{I IFCC}	RF input level for correct IF count	0 to 127		9		dBµVemf
BIT _{IFC}	Counter length			7		Bit
D _{IFC}	Prescaler ratio			64		
t _{IFC GATE}	Gate time	1/(32.768 kHz/400)		12.207		ms
RESIFC	Resolution	64×32.768 kHz/400		5.24288		kHz
NIFC CNT	Count center	325k/64/32.768 kHz × 400		62		Dec
NIFC STOP	IF counter result for search stop		57		67	Dec

ELECTRICAL CHARACTERISTICS – Tx BLOCK

 $V_{CC} = 3 \text{ V}, \text{ } T_A = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF frequency $f_{RF} = 98.1 \text{ MHz}$, BAND = 0 (USEU), MODADJ[3:0] = +6 dB (for 98.1 MHz), Audio signal frequency $f_{AF} = 1 \text{ kHz}$, 100% means FM 75 kdev, BW = LPF 30 k, TxPOW[1:0] = -7 dBm measured with typical home hi-fi tuner (unless otherwise noted)

AF

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
		AFADJ [2:0] = 000	-9		
		AFADJ [2:0] = 001	-6		
		AFADJ [2:0] = 010	-3		
MODD	AE modulation adjust ratio	AFADJ [2:0] = 011 (Ref.)	0		dB
MODR _{AF ADJ}	AF modulation adjust ratio	AFADJ [2:0] = 100	3		uБ
		AFADJ [2:0] = 101	6		
		AFADJ [2:0] = 110	9		
		AFADJ [2:0] = 111	12) - mVpp
	AF maximum input level	AFADJ = 0 dB, EMTC = 0, fs = 400 Hz, L = R each channel		1000	
V _{IMAX 50}	(pre-emphasis 50 μs)	AFADJ = 0 dB, EMTC = 0, fs = 10 kHz, L = R each channel		1000 330 1000 200 15 k	түрр
N	AF maximum input level	AFADJ = 0 dB, EMTC = 1, fs = 400 Hz, L = R each channel		1000	m) (nn
V _{IMAX 75}	(pre-emphasis 75 μs)	AFADJ = 0 dB, EMTC = 1, fs = 10 kHz, L = R each channel		200	mVpp
VIAF	AF yypical input level for 100% dev	$AFADJ = 0 dB$, fs = 400 Hz, $DIS_EM = 0$, L = R each channel	250		mVrms
f _{IAFR}	Input frequency range		20	15 k	Hz
R _{IAF}	AF input impedance		40		kΩ
+	Dro omphosia	EMTC bit = 0	50	1000 200	
t _{PRE}	Pre-emphasis	EMTC bit = 1	75		μs
f _{LPF}	AFLPF frequency response	DIS_AFLPF = 0, -3 dB	15		kHz

Mono Mode

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{O MONO}	Output frequency response	CP = 1.25 μA	20		15 k	Hz
S/N _{MONO98}	Mono signal-to-noise ratio at 98.1 MHz (100% modulation)	$\label{eq:linear} \begin{array}{l} L=R=250 \text{ mVrms}, \ensuremath{f_{AF}}=1 \text{ kHz}, \ensuremath{AFADJ}=0 \text{ dB},\\ MODADJ=5 \text{ dB}, \ensuremath{PLTADJ}=\text{off}, \ensuremath{MONO}\xspace_{ST}=1,\\ RF=98.1 \text{ MHz}, \ensuremath{BAND}=0 \end{array}$		55		dB
THD _{MONO98}	Mono total harmonic distortion at 98.1 MHz (30% modulation)	$\label{eq:linear} \begin{array}{l} L = R = 75 \text{ mVrms}, \ f_{AF} = 1 \text{ kHz}, \ AFADJ = 0 \text{ dB}, \\ MODADJ = 5 \text{ dB}, \ PLTADJ = off, \ MONO_ST = 1, \\ RF = 98.1 \text{ MHz}, \ BAND = 0 \end{array}$	1			%
S/N _{MONO83}	Mono signal-to-noise ratio at 83 MHz (100% modulation)	L = R = 250 mVrms, f_{AF} = 1kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = off, MONO_ST = 1, RF = 83 MHz, BAND = 1	55			dB
THD _{MONO83}	Mono total harmonic distortion at 83 MHz (30% modulation)	$\label{eq:L} \begin{array}{l} L = R = 75 \text{ mVrms}, \ f_{AF} = 1 \text{ kHz}, \ AFADJ = 0 \text{ dB}, \\ MODADJ = 11 \text{ dB PLTADJ} = off, \ MONO_ST = 1, \\ RF = 83 \text{ MHz}, \ BAND = 1 \end{array}$	0.5		%	
ATT _{MT} MONO	MUTE attenuation	MUTE bit = 1	50			dB

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ELECTRICAL CHARACTERISTICS – Tx BLOCK (CONTINUED)

 $V_{CC} = 3 \text{ V}, T_A = 25^{\circ}\text{C}$, measured in the circuit of Figure 26; RF frequency $f_{RF} = 98.1 \text{ MHz}$, BAND = 0 (US/EU), MODADJ[3:0] = +6 dB (for 98.1 MHz), Audio signal frequency $f_{AF} = 1 \text{ kHz}$, 100% means FM 75kdev, BW = LPF 30 k, TxPOW[1:0] = -7 dBm measured with typical home hi-fi tuner (unless otherwise noted)

Stereo Mode

	PARAMETER	TEST CONDITIONS	MIN TYP	MAX	UNIT
S/N _{ST98}	Stereo signal-to-noise ratio at 98.1 MHz Main + Sub = 90%, Pilot = 10%	L = R = 225 mVrms, f_{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = 0 dB, f_{RF} = 98.1 MHz, BAND = 0	55		dB
SEP _{ST98}	Stereo separation at 98.1 MHz Main + Sub = 30%, Pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1 \text{ kHz}$, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = 0 dB, $f_{RF} = 98.1 \text{ MHz}$, BAND = 0	25		dB
THD _{ST98}	Stereo total harmonic distortion at 98.1 MHz Main + Sub = 30%, Pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1 \text{ kHz}$, AFADJ = 0 dB, MODADJ = 5 dB, PLTADJ = 0 dB, $f_{RF} = 98.1\text{MHz}$, BAND = 0	1		%
S/N _{ST83}	Stereo signal-to-noise ratio at 83 MHz Main + Sub = 90%, Pilot = 10%	L = R = 225 mVrms, f_{AF} = 1 kHz, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, f_{RF} = 83 MHz, BAND = 1	55		dB
SEP _{ST83}	Stereo separation at 83 MHz Main + Sub = 30%, Pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1 \text{ kHz}$, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, $f_{RF} = 83 \text{ MHz}$, BAND = 1	30		dB
THD _{ST83}	Stereo total harmonic distortion at 83 MHz Main + Sub = 30%, Pilot = 10%	L or R = 75 mVrms, $f_{AF} = 1 \text{ kHz}$, AFADJ = 0 dB, MODADJ = 11 dB, PLTADJ = 0 dB, $f_{RF} = 83 \text{ MHz}$, BAND = 1	0.5		%
DIFF _{ST MOD}	Left and right channel modulation difference	$\label{eq:linear_state} \begin{array}{l} L = R = 75 \mbox{ mVrms}, f_{AF} = 1 \mbox{ kHz}, \\ AFADJ = 0 \mbox{ dB}, \mbox{ MODADJ} = 11 \mbox{ dB}, \\ PLTADJ = 0 \mbox{ dB}, f_{RF} = 98.1 \mbox{ MHz}, \\ BAND = 1 \mbox{ Lch level ref}. \end{array}$	-1	1	dB

EXT IN

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{EXT MAX}	Maximum input level	EN_EXTIN = 1, DIS_LRIN = 0			500	mVpp
f _{R EXT}	Input frequency range	EN_EXTIN = 1, DIS_LRIN = 0	20		80 k	Hz
V _{OPLT}	Pilot output level	EN_EXTIN = 1, DIS_LRIN = 0		40		mVrms
V _{EXT TYP}	Typical input level for 100% dev	EN_EXTIN = 1, DIS_LRIN = 0		125		mVrms

RF Power

	PARAMETER	TEST CONDITIONS	TYP	UNIT
		TXPOW[1:0] = 00, R_{TX} = open, R_L = 50 Ω , EN_EXTIN = 0, DIS_LRIN = 1	-7	
V	Ty output nowor	TXPOW[1:0] = 01, R_{TX} = 300 Ω , R_L = 50 Ω , EN_EXTIN = 0, DIS_LRIN = 1	-3	dBm
V _{TxOUT} Tx outp	Tx output power	TXPOW[1:0] = 10, R_{TX} = 300 Ω , R_{L} = 50 Ω , EN_EXTIN = 0, DIS_LRIN = 1	1	ubm
		$TXPOW[1:0] = 11, R_TX = 150 \; \Omega, R_L = 50 \; \Omega, EN_EXTIN = 0, DIS_LRIN = 1$	4	

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I²C DATA FORMAT

	Table 1. Rx-Mode Write Data (Address Bit 2, 1 = 0,0)								
BYTE	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	
Address	1	1	0	0	0	0	0	R/W = 0	
Data 1	MUTE	SM	N13	N12	N11	N10	N9	N8	
Data 2	N7	N6	N5	N4	N3	N2	N1	N0	
Data 3	SM_UD	SM_SL1	SM_SL0	LOC_HL	MONO_ST	MUTE_R	MUTE_L	PORT1	
Data 4	PORT2	STBY	BAND	A_MUTE	S_MUTE	HCC	SNC	SM_IND	
Data 5	DIS_EM	EMTC	EN_MPXOUT	0	0	0	CP1	CP0	
Data 6-8		Reserved ⁽¹⁾							

$I^{2}C$ Write Data (R/W = 0)

EXAS RUMENTS

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(1) Do not write any data on reserved area. The data of this area is loaded at power-on-reset.

Table 2. Tx-Mode Write Data (Address Bit 2, 1 = 1,1)

BYTE	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)	
Address	1	1	0	0	0	1	1	R/W = 0	
Data 1	MUTE	0	N13	N12	N11	N10	N9	N8	
Data 2	N7	N6	N5	N4	N3	N2	N1	N0	
Data 3	PLTADJ2	PLTADJ1	PLTADJ0	EN_EXTIN	MONO_ST	TxPOW1	TxPOW0	PORT1	
Data 4	PORT2	STBY	BAND	MODADJ3	MODADJ2	MODADJ1	MODADJ0	DIS_AFLPF	
Data 5	DIS_EM	EMTC	DIS_LRIN	AFADJ2	AFADJ1	AFADJ0	CP1	CP0	
Data 6-8	Reserved ⁽¹⁾								

(1) Do not write any data on reserved area. The data of this area is loaded at power-on-reset.

I^2C Write Data (R/W = 1)

Table 3. Rx-Mode Write Data (Address Bit 2, 1 = 0,0)

					,	- / - /		
BYTE	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Address	1	1	0	0	0	0	0	R/W = 1
Data 1	READY	BAND_LMT	N13	N12	N11	N10	N9	N8
Data 2	N7	N6	N5	N4	N3	N2	N1	N0
Data 3	ST_IND	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0
Data 4	RSSI3	RSSI2	RSSI1	RSSI0	LOCKDET	Х	Х	Х

Table 4.	Tx-Mode	Write Data	(Address	Bit 2, 1 = 1,1)
----------	---------	------------	----------	-----------------

					•			
BYTE	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Address	1	1	0	0	0	1	1	R/W = 1
Data 1	0	0	N13	N12	N11	N10	N9	N8
Data 2	N7	N6	N5	N4	N3	N2	N1	N0
Data 3	ST_IND	1	1	1	1	1	1	1
Data 4	1	1	1	1	Х	1	1	1

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Table 5. Rx-Mode Write Data	Symbol Description	$(\Delta ddress Bit 2 1 = 0.0)$
Table J. INA-INIQUE WITTLE Data	Symbol Description	(Auu = 55 Dit 2, 1 = 0,0)

SYMBOL		DESCRIPTION	DEFAULT
MUTE	Mute control bit	0: Mute off 1: Mute on	0
SM	Search mode control bit	0: Off 1: On (start search when 0 to 1)	0
N13–N0	Programmable counter bits	Set main counter	All 0
SM_UD	Search up/down set bit	0: Down 1: Up	1
SM_SL1, SM_SL0	Search stop-level bits	$\begin{tabular}{ c c c c } \hline SM_L1 & SM_L0 & RSSI Level \\ \hline 0 & 0 & \geq 0 \mbox{ (test function)} \\ \hline 0 & 1 & \geq 5 \\ \hline 1 & 0 & \geq 8 \\ \hline 1 & 1 & \geq 12 \\ \hline \end{tabular}$	1, 1
LOC_HL	Local high-/low-side injection control bit	0: Low-side LO injection 1: High-side LO injection	1
MONO_ST	Mono/stereo switch	0: Auto stereo 1: Forced mono	0
MUTE_R, MUTE_L	R-ch mute switch, L-ch mute switch	0: Mute off 1: Mute on	0, 0
PORT1	Port 1 control bit	PORT 1 is enable as general purpose port in condition of SM_IND = 0 0: Low (Nch-MOS open drain on) 1: High (Nch-MOS open drain off) When SIM_IND = 1, PORT 1 outputs search indicator.	1
PORT2	Port 2 control bit	0: Low (open drain on) 1: High (open drain off)	1
STBY	Standby control bit	0: Standby off 1: Standby on	1
BAND	Band selection at search mode	0: US/EU band (87.5 MHz to 108 MHz) 1: Japan band (76 MHz to 90 MHz)	0
A_MUTE	Auto mute control bit	0: Off 1: On (auto mute when PLL unlocked or search mode)	0
S_MUTE	Soft mute control bit	0: Off 1: On	0
HCC	High cut control bit	0: Off 1: On	0
SNC	Stereo noise cancel bit	0: Off 1: On	0
SM_IND	Search indicator control bit	0: Disable indicator. Port 1 is controlled by bit PORT1.1: Enable indicator. Port1 outputs as search indicator (in search sequence: L, Normal operation: H).	0
DIS_EM	Disable De-emphasis bit	0: De-emphasis on 1: De-emphasis off	0
EMTC	Time constant control bit for De-emphasis	0: 50 μs 1: 75 μs	1
EN_MPXOUT	MPX output control bit	0: Output disable 1: Output enable	0
CP1, CP0	CP current selection bit 1, CP current selection bit 0	CP1 CP0 CP Current 0 0 0.6 μA 0 1 1.25 μA 1 0 2.5 μA 1 1 5 μA	1, 0

SYMBOL			DESCRI	PTION			DEFAULT
MUTE	Mute control bit	0: Mute off 1: Mute on					0
N13–N0	Programmable counter bits	Set main co	unter				All 0
PLTADJ2,	Pilot-level adjust bits	PLT	ADJ2	PLTADJ1	PLTADJ0	Level	0,
PLTADJ1, PLTADJ0			0 0 0 1 1 1 1 1 1	0 0 1 1 0 0 1 1 0 0 4B = 1 = B =	0 1 0 1 0 1 0 1 10% of 250 mVr	6 dB 4 dB 2 dB 0 dB 2 dB 4 dB 6 dB Pilot off	1, 1
EN_EXTIN	EXT input enable bit	0: Disable E	XT IN, PLT OU XT IN, PLT OU	JT	10/0 01 200 1111		0
MONO_ST	Mono/stereo switch	0: 38 kHz su 1: 38 kHz su	bcarrier on		set as PLTADJ[2	:0] = 111	0
TxPOW1,	Tx power-level selection		TxPOW1		TxPOW0	Level	0,
TxPOW0	bits		0 0 1 1		0 1 0 1	7 dBm 3 dBm 1 dBm 4 dBm	0
PORT1, PORT2	Port 1 control bit, Port 2 control bit	0: Low (Nch	PORT2 are er -MOS open dra -MOS open dr	ain on)	al purpose ports.		1, 1
STBY	Standby control bit	0: Standby of 1:					1
BAND	Band selection at search mode		and (87.5 MHz nd (76 MHz to				0
MODADJ3, MODADJ2,	Modulation adjust bits	MODADJ3	MODADJ2	MODADJ1	MODADJ0	Total Composite Level	
MODADJ1, MODADJ0		0 0 0 0 0 0 1 1 1 1 1 1 1	0 0 1 1 1 1 0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	0 dB 1 dB 2 dB 3 dB 4 dB 5 dB 6 dB 7 dB 8 dB 9 dB 10 dB 11 dB 12 dB 13 dB 14 dB 15 dB	
DIS_AFLPF	Disable 15-kHz LPF		z LPF enable z LPF disable				0
DIS_EM	Disable pre-emphasis bit	0: Pre-emph 1: Pre-emph					0
EMTC	Time constant control bit for pre-emphasis	0: 50 μs 1: 75 μs					1
DIS_LIN, DIS_RIN	MPX output control bit	0: Output dis 1: Output er					0

Table 6. Tx-Mode Write Data Symbol Description (Address Bit 2, 1 = 1,1)

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Table 6. Tx-Mode Write Data Symbol Description (Address Bit 2, 1 = 1,1) (continued)

SYMBOL		DESC	CRIPTION			DEFAULT
AFADJ2,	AF-level adjust bits	AFADJ2	AFADJ0	AFADJ1	Level	0,
AFADJ1,		0	0	0	–9 dB	1,
AFADJ0		0	0	1	–6 dB	1
		0	1	0	–3 dB	
		0	1	1	0 dB	
		1	0	0	3 dB	
		1	0	1	6 dB	
		1	1	0	9 dB	
		1	1	1	12 dB	
CP1,	CP current selection bit 1,	CP1	CP0	CF	Current	1,
CP0	CP current selection bit 0	0	0	(0.6 μΑ	0
		0	1		.25 μA	
		1	0		2.5 μÅ	
		1	1		5 μA	

Table 7. Rx-Mode Read Data Symbol Description (Address Bit 2, 1 = 0,0)

SYMBOL		DESCRIPTION	
READY	Ready flag	0: PLL unlocked or search operation 1: Normal operation	
BAND_LMT	Band limit flag at end of search operation	0: Not reached band limit (found station) 1: Reached band limit (not found station) (reset to 0 when I ² C date write)	
N13-N0	Programmable counter bits	Setting of counter after search	
ST_IND	Stereo indicator bit	0: Mono reception 1: Stereo reception	
IFC6–0	IF counter result bits	IF counter result (0 to 127 dec) Step frequency = $(64 \times 32.768 \text{ k})/400 = 5.24288 \text{ k}$ (Hz)	
RSSI3-0	RSSI level bits	RSSI level (0 to 15 dec)	
LOCKDET	Lock detect flag	0: Unlocked 1: Locked	

Table 8. Tx-Mode Read Data Symbol Description (Address Bit 2, 1 = 1,1)

SYMBOL	DESCRIPTION					
N13–N0	Programmable counter bits	Setting of main counter				
ST_IND	Stereo indicator bit	0: Stereo modulation 1: Other status				

Table 9. Examples of Tx Mode Adjustment Bit Settings⁽¹⁾

BAND	Tx FREQUENCY (MHz)	MODADJ LEVEL ⁽²⁾ (dB)	MODADJ BIT[3:0]	AFADJ LEVEL ⁽³⁾ (dB)	AFADJ BIT[2:0]	PLTADJ LEVEL (dB)	PLTADJ BIT[2:0]
US/EU	87.5	9	1001	0	011	0	011
US/EU	108	3	0011	0	011	0	011
JP	76	13	1101	0	011	0	011
JP	90	8	1000	0	011	0	011

(1) These settings are to obtain audio modulation level of 22.5 kHzdev (30% modulation) and pilot level of 7.5 kHzdev (10% modulation) when audio input level = 75 mVrms and audio input frequency = 400 Hz.

(2) An adequate level for each Tx frequency should be selected for MODADJ. See Figure 33 and Figure 34.

(3) AFADJ should be adjusted to maintain audio level × adjust level (dB) less than 250 mVrms. For example, when audio input level for 100% modulation is 500 mVrms, AFADJ should be –6 dB (AFADJ[2:1] = 001).



PLL Setting

N13–N0 14-bit word (NPLL) can be calculated as follows:

f_{IF}= IF frequency (325 kHz)

f_{RF} = Wanted tuning frequency

 f_{IXTAL} = Crystal frequency (32.768 kHz)

F	Тх	
Upper Local Setting	Lower Local Setting	IX
$N_{PLL} = 4 \times \frac{f_{RF} + f_{IF}}{f_{XTAL}}$	$N_{PLL} = 4 \times \frac{f_{RF} - f_{IF}}{f_{XTAL}}$	$N_{PLL} = 4 \times \frac{f_{RF}}{f_{XTAL}}$

Example for Rx mode:

 $f_{RF} = 81.3 \text{ MHz}$, lower local

 $N_{PLL} = 4 \times \frac{81.3M - 325k}{32.768} = 9885$

The PLL word becomes 269Dh (N[13:0] = 10 0110 1001 1101).

Example for Tx mode:

 $f_{RF} = 88 \text{ MHz}$

 $N_{PLL} = 4 \times \frac{88M}{32.768k} = 10742$

The PLL word becomes 29F6h (N[13:0] = 10 1001 1111 0110).

Standby Mode

Standby mode can be controlled by STBY pin voltage and STBY bit data as shown in Table 10.

Table 10. Standby Mode

VOLTAGE APPLIED ON STBY PIN	I ² C STBY BIT DATA	DEVICE OPERATION
L	0	Standby
L	1	Standby
Н	0	Normal Operation
Н	1	Standby

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FM Transmitter Block

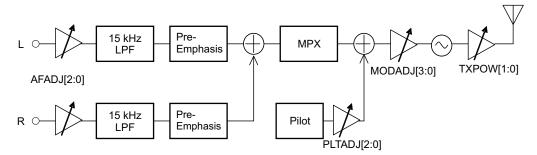
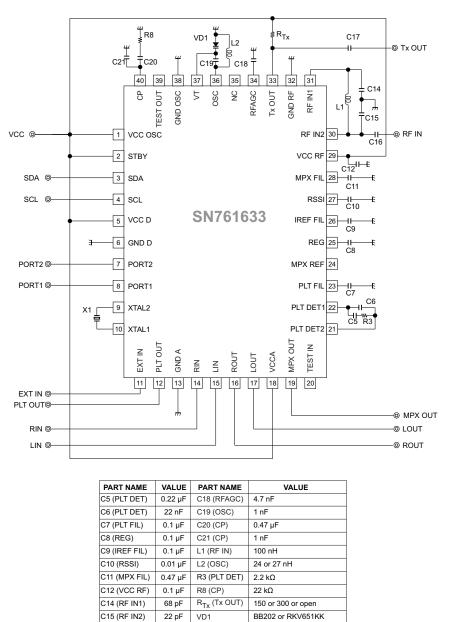


Figure 25. FM Transmitter Block Diagram

Initial setting	Audio input level:	L = R = 75 mVrms, AFADJ = 0 dB, fs = 400 Hz				
	Pilot level:	PLTADJ = 0 dB means 10%				
	FM modulation:	MODADJ depends on Tx frequency to be 22.5 kHz dev.				
	Output power:	TxPOW = -7 dBm	Pullup resistance is not necessary.			
		TxPOW =–3, 1 dB	Antenna load 50 Ω add pullup resistance R_{TX} 300 Ω			
		TxPOW = 4 dBm	Antenna load 50 Ω add pullup resistance R_{TX} 150 Ω			

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APPLICATION INFORMATION



A. This application information is advisory and a performance check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents of third parties.

X1

C16 (RF IN2)

C17 (Tx OUT)

330 pF

0.01 µF

Figure 26. Application Circuit

32.768 kHz, C_L = 12.5 pF

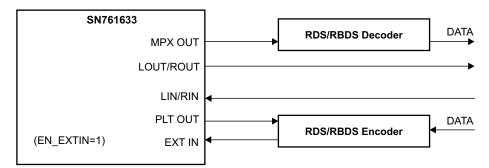
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RDS Solution





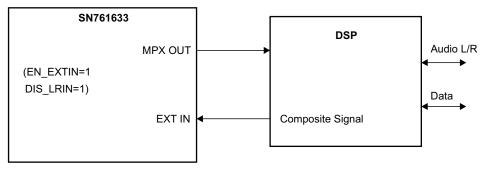
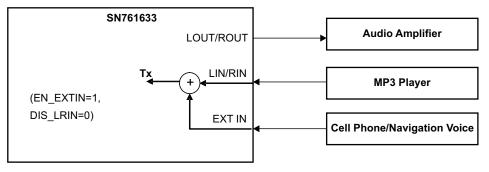


Figure 28. RDS Solution 2 (DSP Interface)

Mixing Mode (Tx)

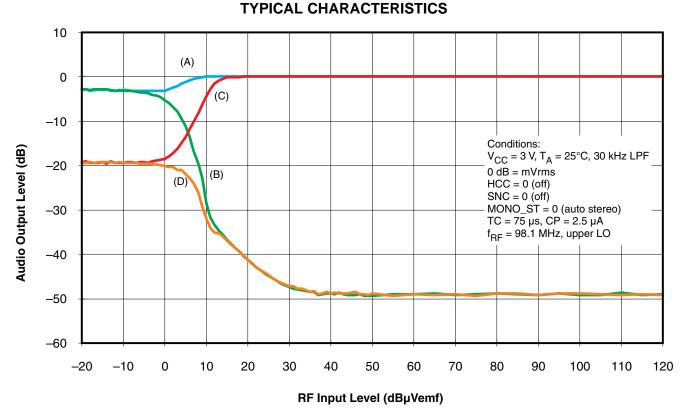
LIN/RIN and EXT IN signals can be mixed as a Tx signal.







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A. Mono signal, soft mute off (f_{AF} = 1 kHz, 22.5 kHz dev, 30%)

B. Noise in mono mode, soft mute off

TEXAS IRUMENTS

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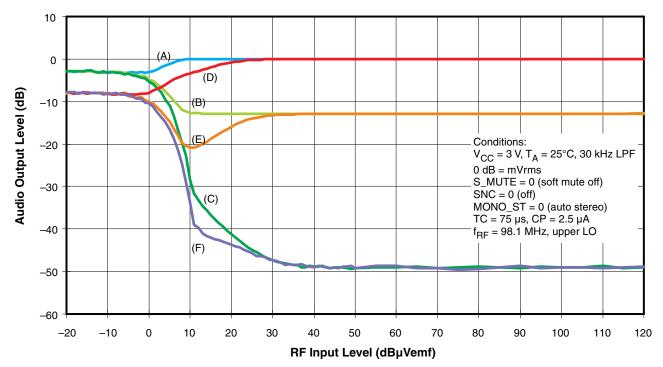
- C. Mono signal, soft mute on (f_{AF} = 1 kHz, 22.5 kHz dev, 30%)
- D. Noise in mono mode, soft mute on

Figure 30. Rx-Mode FM Mono Characteristics (Soft Mute On/Off)

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TYPICAL CHARACTERISTICS (continued)



A. Mono signal, high cut off (f_{AF} = 1 kHz, 22.5 kHz dev, 30%)

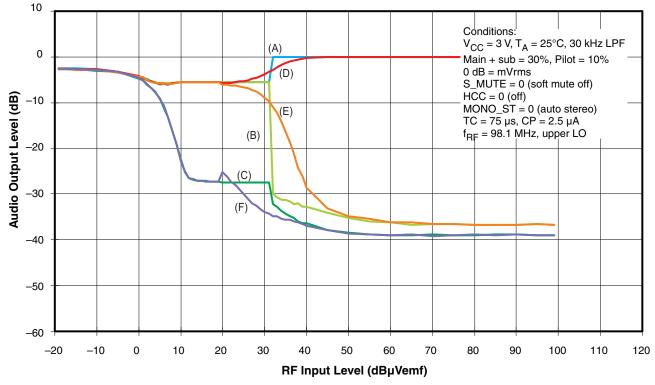
- B. Mono signal, high cut off (f_{AF} = 10 kHz, 22.5 kHz dev)
- C. Noise in mono mode, high cut off
- D. Mono signal, high cut on (f_{AF} = 1 kHz, 22.5 kHz dev, 30%)
- E. Mono signal, high cut on (f_{AF} = 10 kHz, 22.5 kHz dev)
- F. Noise in mono mode, high cut on

Figure 31. Rx-Mode FM Mono Characteristics (High Cut Control [HCC] On/Off)



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A. Stereo left signal, noise control off (f_{AF} = 1 kHz, 22.5 kHz dev)

B. Stereo right signal, noise control off (audio signal off)

C. Noise in stereo mode, noise control off

D. Stereo left signal, noise control on (f_{AF} =1 kHz, 22.5 kHz dev)

E. Stereo right signal, noise control on (audio signal off)

F. Noise in stereo mode, noise control cut on

Figure 32. Rx-Mode FM Stereo Characteristics [Stereo Noise Control (SNC) On/Off]

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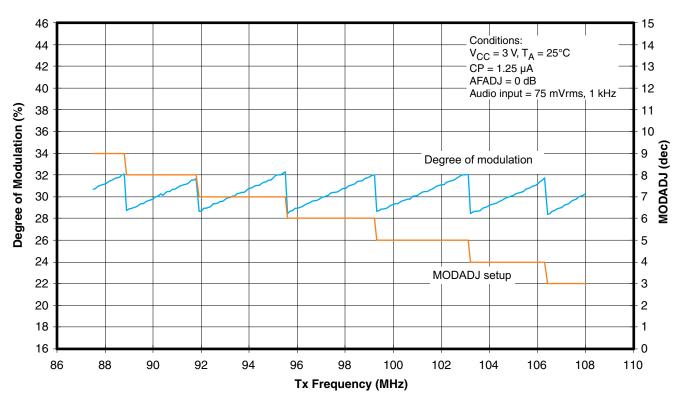
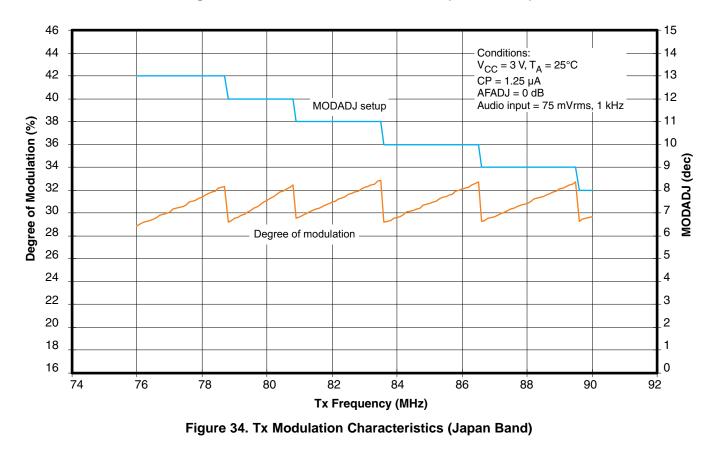


Figure 33. Tx Modulation Characteristics (US/EU Band)





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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
SN761633RTAR	OBSOLETE	WQFN	RTA	40		TBD	Call TI	Call TI	-20 to 85	SN76 1633	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

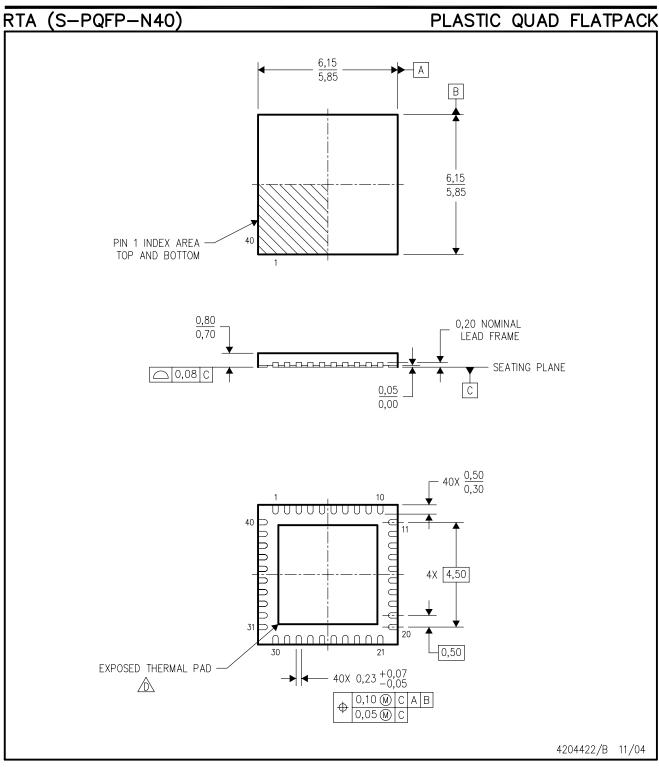
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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MECHANICAL DATA



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- A The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



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