ATSAMB11XR/ZR

Ultra-Low Power Bluetooth® Low Energy SiP/Module

Introduction

The ATSAMB11-XR2100A is an ultra-low power Bluetooth Low Energy (BLE) 4.2 System in a Package (SiP) with Integrated MCU, transceiver, modem, MAC, PA, Transmit/Receive (T/R) switch, and Power Management Unit (PMU). It is a standalone Cortex® -M0 applications processor with embedded Flash memory and BLE connectivity.

The Bluetooth SIG-qualified Bluetooth Low Energy protocol stack is stored in a dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, example applications are available for application profiles such as proximity, thermometer, heart rate and blood pressure, and many others.

The ATSAMB11-XR2100A provides a compact footprint and various embedded features, such as a 26 MHz crystal oscillator.

The ATSAMB11-ZR210CA is a fully certified module that contains the ATSAMB11-XR2100A and all external RF circuitry required, including a ceramic high-gain antenna. The user simply places the module into their PCB and provides power with a 32.768 kHz Real-Time Clock (RTC) or crystal, and an I/O path.

Microchip BluSDK Smart offers a comprehensive set of tools and reference applications for several Bluetooth SIG defined profiles and a custom profile. The BluSDK Smart will help the user quickly evaluate, design and develop BLE products with the ATSAMB11-XR2100A and ATSAMB11-ZR210CA.

The ATSAMB11-XR2100A and associated ATSAMB11-ZR210CA module have passed the Bluetooth SIG certification for interoperability with the Bluetooth Low Energy 4.2 specification.

Features

- 2.4 GHz Transceiver and Modem:
  - -92.5 dBm receiver sensitivity
  - -55 dBm to +3.5 dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection (ATSAMB11-XR2100A)
  - Incorporated chip antenna (ATSAMB11-ZR210CA)
- Processor Features:
  - ARM® Cortex®-M0 32-bit processor
  - Serial Wire Debug (SWD) interface
  - Four-channel Direct Memory Access (DMA) controller
  - Watchdog timer
- Memory:

  - 128 KB embedded Random Access Memory (RAM)
  - 128 KB embedded ROM
  - 256 KB stacked Flash memory
- Hardware Security Accelerators:
  - Advanced Encryption Standard (AES)-128
  - Secure Hash Algorithm (SHA)-256
- Peripherals:
  - 23 digital and 4 mixed-signal General Purpose Input Outputs (GPIOs) with 96 kOhm internal programmable pull-up or down resistors and retention capability, and one wake-up GPIO with 96 kOhm internal pull-up resistor
  - Two Serial Peripheral Interface (SPI) Master/Slave
  - Two Inter-Integrated Circuit (I^2C) Master/Slave
  - Two UART
  - One SPI flash interface (used for accessing the internal stacked flash)
  - Three-axis quadrature decoder
  - Four Pulse Width Modulation (PWM) channels
  - Three General Purpose Timers and one Always-On (AON) sleep Timer
  - 4-channel, 11-bit Analog-to-Digital Converter (ADC)
- Clock:
  - Integrated 26 MHz RC oscillator
  - Integrated 2 MHz RC oscillator
  - 26 MHz crystal oscillator (XO)
  - 32.768 kHz Real Time Clock crystal oscillator (RTC XO)
- Ultra-Low Power:
  - 2.03 µA sleep current
  - 4.17 mA peak TX current (1)
  - 5.26 mA peak RX current
  - 16.4 µA average advertisement current (three channels, 1s interval) (2)
- Integrated Power Management:
  - 2.3V to 4.3V battery voltage range
  - 2.3V to 3.6V input range for I/O (limited by Flash memory)
  - Fully integrated Buck DC/DC converter
- Temperature Range:
  - -40°C to 85°C
- Package:
  - 49-pin FLGA SiP package 5.50 mm x 4.50 mm
  - 35-pin module package 10.541 mm x 7.503 mm

Note:

1. TX output power - 0 dBm.
2. Advertisement channels - 3 ; Advertising interval - 1 second ; Advertising event type - Connectable undirected; Advertisement data payload size - 31 octets.

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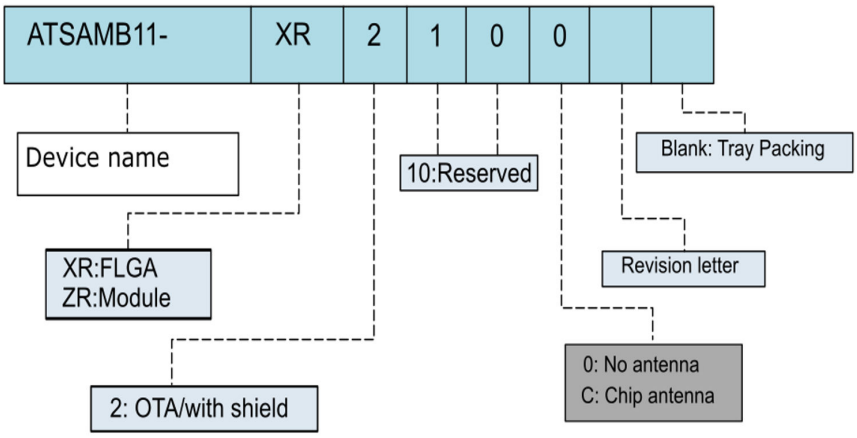
1. Ordering Information

Table 1-1. Ordering Details

Model Number	Ordering Code	Package	Description	Regulatory Information
ATSAMB11-XR2100A	ATSAMB11-XR2100A	5.5 mm x 4.5 mm	ATSAMB11 SiP tray	N/A
ATSAMB11-ZR210CA	ATSAMB11-ZR210CA	7.5 mm X 10.5 mm	ATSAMB11 module with chip antenna	FCC, ISED, CE

Figure 1-1. Marking information



2. Package Information

Table 2-1. ATSAMB11-XR2100A SiP 49 Package Information

Parameter	Value	Units	Tolerance
Package size	5.50 x 4.50	mm	±0.05 mm
Pad count	49		
Total thickness	1.40	mm	Max
Tolerance (maximum pad pitch)	0.40	mm	±0.05 mm
Pad width	0.21		
Exposed pad size	0.50 x 0.50		

Note: For drawing details, see Figure 18-1.

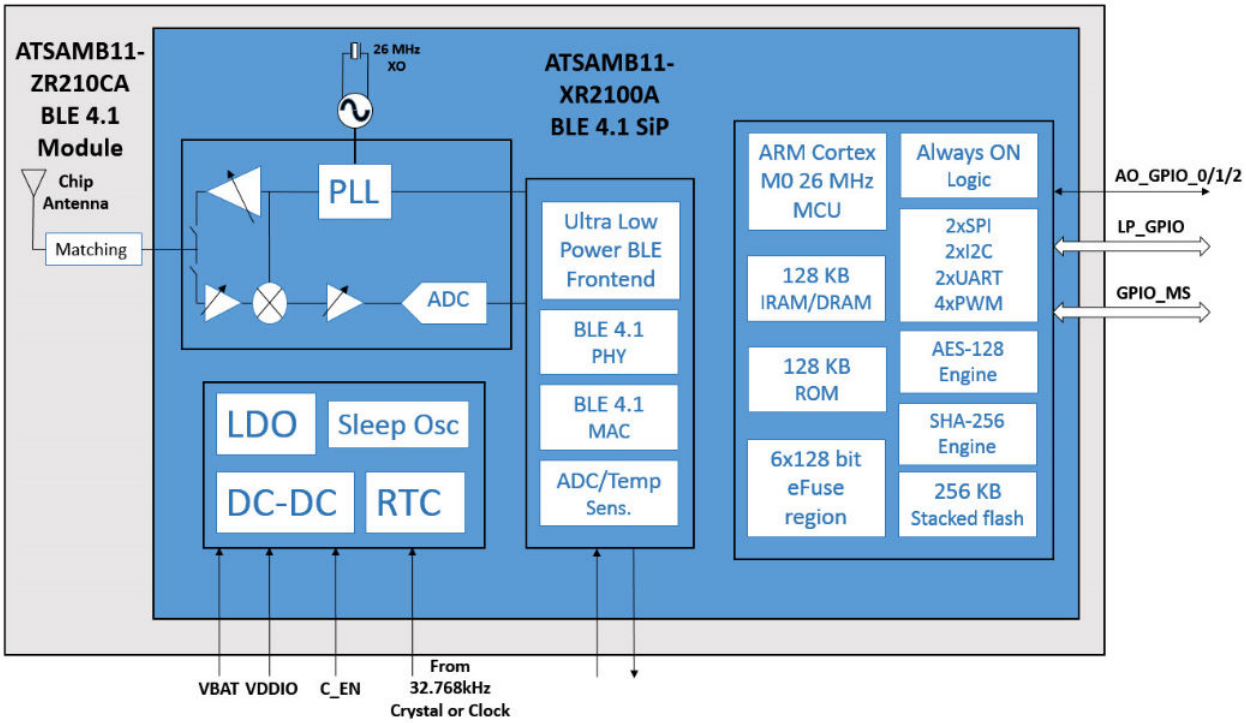
Table 2-2. ATSAMB11-ZR210CA Module Information

Parameter	Value	Units	Tolerance
Package size	7.503 x 10.541	mm	Untoleranced dimension
Pad count	35		
Total thickness	1.868	mm	Untoleranced dimensions
Pad pitch	0.61		
Pad width	0.406		
Exposed pad size	2.705 x 2.705		

Note: For drawing details, see Figure 18-2.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pinout Information

The ATSAMB11-XR2100A is offered in an exposed pad 49-pin SiP package. This package has an exposed paddle that must be connected to the system board ground. The SiP package pin assignment is shown in the figure below. The colored shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The ATSAMB11-ZR210CA module is a castellated PCB with the ATSAMB11-XR2100A integrated with a matched chip antenna. The pins are identified in the pin description table. The ATSAMB11-XR2100A also contains a paddle pad on the bottom of the PCB, that must be soldered to the system ground.

Figure 4-1. ATSAMB11-XR2100A Pin Assignment

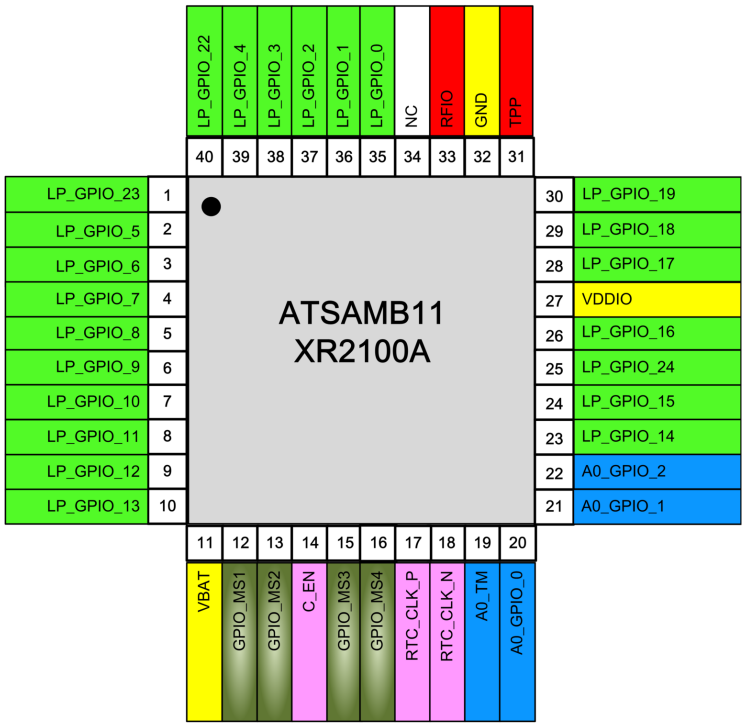
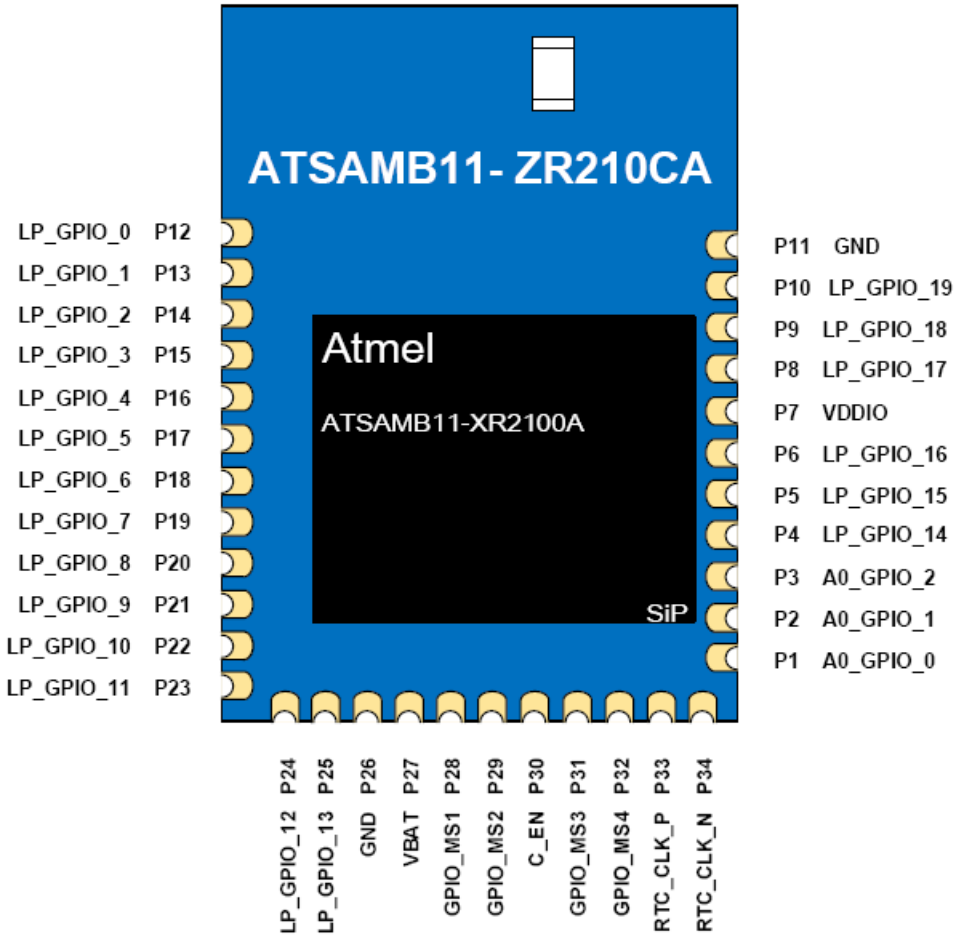


Figure 4-2. ATSAMB11-ZR210CA Pin Descriptions



The following table lists the pin assignments for both the ATSAMB11-XR2100A and the ATSAMB11-ZR210CA.

Table 4-1. ATSAMB11-XR2100A and ATSAMB11-ZR210CA Pin Description

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
1	-	LP_GPIO_23	Digital I/O	GPIO with Programmable Pull Up/Down
2	17	LP_GPIO_5	Digital I/O	GPIO with Programmable Pull Up/Down
3	18	LP_GPIO_6	Digital I/O	GPIO with Programmable Pull Up/Down
4	19	LP_GPIO_7	Digital I/O	GPIO with Programmable Pull Up/Down
5	20	LP_GPIO_8(1)	Digital I/O	GPIO with Programmable Pull Up/Down

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
6	21	LP_GPIO_9(1)	Digital I/O	GPIO with Programmable Pull Up/Down
7	22	LP_GPIO_10	Digital I/O	GPIO with Programmable Pull Up/Down
8	23	LP_GPIO_11	Digital I/O	GPIO with Programmable Pull Up/Down
9	24	LP_GPIO_12	Digital I/O	GPIO with Programmable Pull Up/Down
10	25	LP_GPIO_13	Digital I/O	GPIO with Programmable Pull Up/Down
11	27	VBAT	Power supply	Power supply pin for the DC/DC convertor
12	28	GPIO_MS1	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
13	29	GPIO_MS2	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
14	30	C_EN	Digital Input	Can be used to control the state of PMU. High level enables the module; low-level places module in Power-Down mode.
15	31	GPIO_MS3	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
16	32	GPIO_MS4	Mixed Signal I/O	Configurable to be a GPIO digital and analog signal. Only analog input for ADC interface.
17	33	RTC_CLK_P	Analog	Crystal pin or External clock supply, see 32.768 kHz RTC Crystal Oscillator (RTC XO)
18	34	RTC_CLK_N	Analog	Crystal pin or External clock supply, see 32.768 kHz RTC Crystal Oscillator (RTC XO)
19	-	AO_TM	Digital Input	Always-On Test Mode. Connect to GND

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
20	1	AO_GPIO_0	Always On Digital I/O, Programmable Pull-Up	To be held in logic '0' GND to allow the device to enter Ultra_Low_Power mode Can be used to Wake-up the device from Ultra_Low_Power mode.
21	2	AO_GPIO_1	Always On. Digital I/O, Programmable Pull- Up	GPIO with Programmable Pull Up
22	3	AO_GPIO_2	Always On. Digital I/O, Programmable Pull- Up	GPIO with Programmable Pull Up
23	4	LP_GPIO_14	Digital I/O	GPIO with Programmable Pull Up/Down
24	5	LP_GPIO_15	Digital I/O	GPIO with Programmable Pull Up/Down
25	-	LP_GPIO_24	Digital I/O	GPIO with Programmable Pull Up/Down
26	6	LP_GPIO_16	Digital I/O	GPIO with Programmable Pull Up/Down
27	7	VDDIO	Power supply	Power supply pin for the I/O pins. Can be less than or equal to voltage supplied at VBAT
28	8	LP_GPIO_17	Digital I/O	GPIO with Programmable Pull Up/Down
29	9	LP_GPIO_18	Digital I/O	GPIO with Programmable Pull Up/Down
30	10	LP_GPIO_19	Digital I/O	GPIO with Programmable Pull Up/Down
31	-	TPP		Do not connect
32	11, 26	GND	Ground	
33	-	RFIO	Analog I/O	RX input and TX output. Single-ended RF I/O; To be connected to antenna
34	-	NC		Do not connect
35	12	LP_GPIO_0	Digital I/O	SWD clock

ATSAMB11-XR2100A Pin #	ATSAMB11-ZR210CA Pin #	Pin Name	Pin Type	Description / Default Function
36	13	LP_GPIO_1	Digital I/O	SWD I/O
37	14	LP_GPIO_2	Digital I/O	GPIO with Programmable Pull Up/Down
38	15	LP_GPIO_3	Digital I/O	GPIO with Programmable Pull Up/Down
39	16	LP_GPIO_4	Digital I/O	GPIO with Programmable Pull Up/Down
40	-	LP_GPIO_22	Digital I/O	GPIO with Programmable Pull Up/Down
41 - 49	35	Paddle	Ground	Exposed paddle must be soldered to system ground

Note:

1. These GPIO pads are high-drive pads. Refer Table 17-3.

5. Device States

This section includes details on the description and controlling of the Device states.

5.1 Description of Device States

The ATSAMB11-XR2100A and the ATSAMB11-ZR210CA have multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered on, if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal.
- BLE_On_Receive – Device is in active receive state.
- MCU_Only – Device has ARM processor powered-on and BLE subsystem powered-down.
- Ultra_Low_Power – BLE subsystem and ARM processor are powered-down.
- Power_Down – Device core supply off.

5.1.1 Controlling the Device States

The following pins are used to switch between the main device states:

- C_EN – used to enable PMU
- VDDIO – I/O supply voltage from an external power supply
- AO_GPIO_0 - can be used to control the device from entering/exiting Ultra_Low_Power mode

To be in the Power_Down state, the VDDIO supply must be turned on and the C_EN must be maintained at logic low (at GND level). To switch between the Power_Down state and the MCU_Only state, C_EN is to be maintained at logic high (VDDIO voltage level). Once the device is in the MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO supply is turned off and C_EN is in logic low, the chip is powered off with no leakage.

When VDDIO supply is turned off, voltage cannot be applied to the ATSAMB11-XR2100A pins, as each pin contains an ESD diode from the pin to supply. This diode turns on, when a voltage higher than one diode-drop is supplied to the pin.

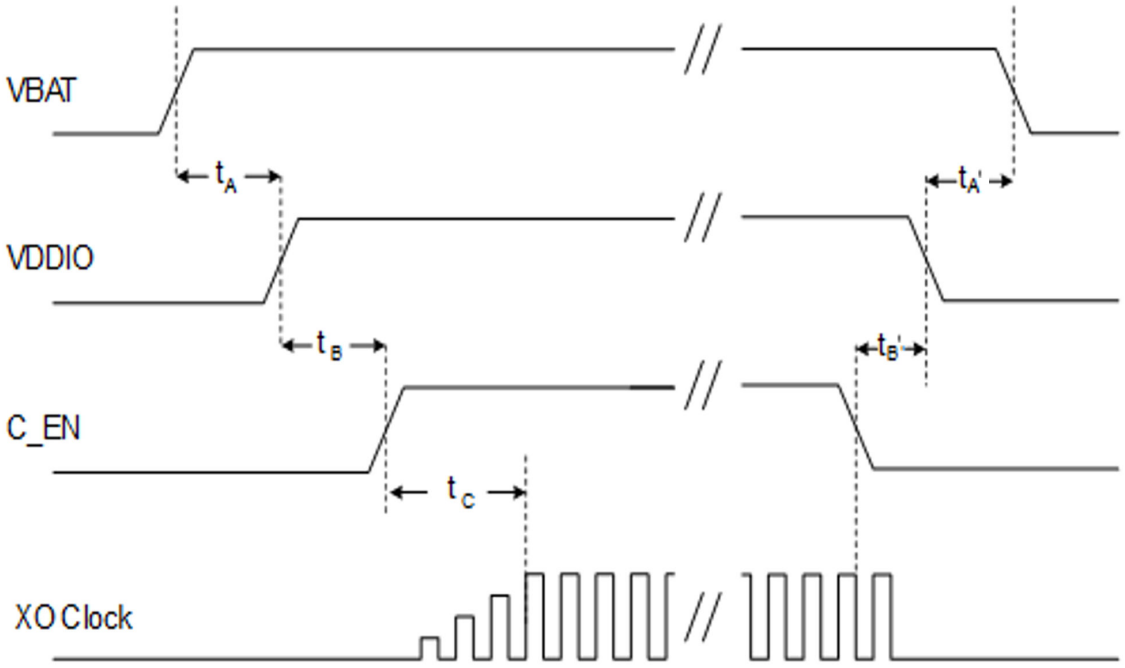
If voltage is to be applied to the signal pads, while the chip is in a low-power state, the VDDIO supply must be on, so that the Power_Down state is used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage to any pin that is more than one diode-drop below ground.

The AO_GPIO_0 pin can be used to control the device from entering and exiting Ultra_Low_Power mode. When AO_GPIO_0 is maintained in logic high state, the device will not enter Ultra_Low_Power mode. When the AO_GPIO_0 is maintained in logic low, the device will enter Ultra_Low_Power mode provided there are no BLE events to be handled.

5.2 Power Sequences

The power sequences and timing parameters for the ATSAMB11-XR2100A and ATSAMB11-ZR210CA, are illustrated below.

Figure 5-1. Power-up/Power-down Sequence



The timing parameters are provided in following table.

Table 5-1. Power-up/Power-down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or can be tied together
t_B	0			VDDIO rise to C_EN rise	C_EN must not rise before VDDIO. C_EN must be driven high or low, not left floating.
t_C	10		µs	C_EN rise to 31.25 kHz (2 MHz/64) oscillator stabilizing	
$t_{B'}$	0		ms	C_EN fall to VDDIO fall	C_EN must fall before VDDIO. C_EN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBAT fall	VBAT and VDDIO can fall simultaneously or be tied together

5.3 Digital and Mixed-Signal I/O Pin Behavior during Power-Up Sequences

The following table represents I/O pin states corresponding to device power modes.

Table 5-2. I/O Pin Behavior in the Different Device States (1)

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor (2)
Power_Down: core supply off	High	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-on Reset: core supply on, POR hard reset pulse on	High	High	Disabled (Hi-Z)	Disabled	Disabled (3)
Power-on Default: core supply on, device out of reset but not programmed yet	High	High	Disabled (Hi-Z)	Enabled(4)	Enabled Pull-Up (4)
MCU_Only, BLE_On: core supply on, device programmed by firmware	High	High	Programmed by firmware for each pin: Enabled or Disabled (Hi-Z) (5) ,when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled (5)	Programmed by firmware for each pin: Enabled or Disabled, Pull-Up or Pull- Down(5)
Ultra_Low_Power: core supply on for always-on domain, core supply off for switchable domains	High	High	Retains previous state(6) for each pin: Enabled or Disabled (Hi-Z), when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled(6)	Retains previous state (6) for each pin: Enabled or Disabled, Pull-Up or Pull-Down

Note:

1. This table applies to all three types of I/O pins (digital switchable domain GPIOs, digital always-on/wake-up GPIO, and mixed-signal GPIOs) unless otherwise noted.
2. Pull-up/down resistor value is 96 kOhm ±10%.
3. In Power-on Reset state, the pull-up resistor is enabled in the always-on/wake-up GPIO only.
4. In Power-on Default state, the input drivers and pull-up/down resistors are disabled in the mixed-signal GPIOs only (mixed-signal GPIOs are defaulted to analog mode, see the note below).
5. Mixed-signal GPIOs can be programmed to be in analog or digital mode for each pin: when programmed to analog mode (default), the output driver, input driver, and pull-up/down resistors are all disabled.
6. In Ultra_Low_Power state, the always-on/wake-up GPIO does not have retention capability and behaves same as in MCU_Only or BLE_On states, also for mixed-signal GPIOs programming analog mode overrides retention functionality for each pin.

6. Processor Architecture

6.1 ARM Subsystem

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

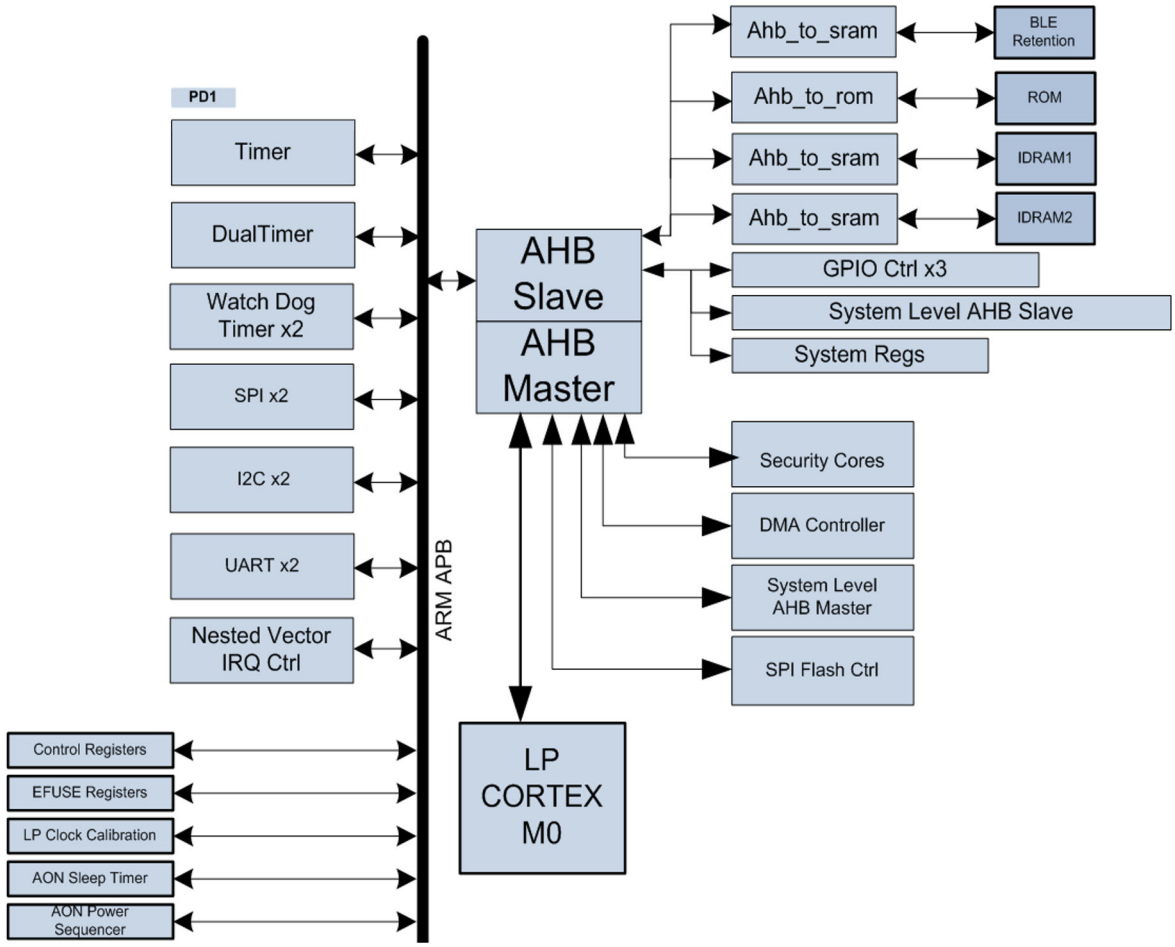
The Cortex-M0 Microcontroller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution with four hardware breakpoint and two watchpoint options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

ATSAMB11 is running a proprietary RTOS tightly coupled with FW in the ROM and the user can not override it. SysTick timer is being used by the stack and will not be available for usage by the application.

Figure 6-1. ARM Cortex-M0 Subsystem



6.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic and high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

6.1.2 Wakeup Sources

Ultra_Low_Power is the lowest possible power state for the system. In Ultra_Low_Power state, ARM Cortex-M0, BLE core, GPIO's, and all other peripheral cores are powered-down. Only AON-GPIO_0 and AON-Sleep timer are functional in this state.

ATSAMB11 contains the following wake-up sources that wake up the system from Ultra_Low_Power mode:

- BLE events
- AON-GPIO_0
- AON-Sleep timer

6.2 Cortex M0 Peripherals

- System Control Space (SCS)
  The processor provides debug through registers in the SCS. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- Nested Vectored Interrupt Controller (NVIC)
  External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- System Timer (SysTick)
  The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. For more details, refer to the Cortex-M0 Technical Reference Manual (http://www.arm.com).
- System Control Block (SCB)
  The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. For more details, refer to the Cortex-M0 Devices Generic User Guide (http://www.arm.com).

6.2.1 Cortex M0 Peripheral Memory Map

- 0xE000E000 System Control Space (SCS)
- 0xE000E010 System Timer (SysTick)
- 0xE000E100 Nested Vectored Interrupt Controller (NVIC)
- 0xE000ED00 System Control Block (SCB)

6.3 Nested Vector Interrupt Controller

External interrupt signals are connected to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled to provide low-latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little endian. Any attempt to read or write a half-word or byte individually is unpredictable.

The NVIC allows the CPU to be able to individually enable or disable each interrupt source, and hold each interrupt until it is serviced and cleared by the CPU.

Table 6-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

Note: For a description of each register, see the Cortex-M0 documentation from ARM (http://www.arm.com).

6.3.1 Functional Description

The Cortex-M0 NVIC is connected to 32 IRQ sources. The following table lists the interrupts that are available in ATSAMB11. Also, some of the interrupts are marked as RESERVED as they are used by the BLE stack and are used for firmware in general. Applications must refrain from registering an ISR for those interrupts as it affects the chip functionality.

Perform the following steps to enable an interrupt:

- Configure and enable peripheral interrupt using peripheral-specific registers. Refer to the intended peripheral chapter for configuring interrupt.
- The ISRs are mapped in RAM memory called interrupt vector table. 0x10000000 is the start address of first ISR index 0 and 4 bytes are allocated for each ISR index in incrementing order. The specific peripheral ISR handler to be registered by assigning the handler address to this interrupt vector table.
- Set the NVIC priority of the interrupt if required. IPR0-IPR7 ARM NVIC registers are used to set the priority level for individual interrupt sources. IRQ number of the specific interrupt source as per the following table is used. Only two bits are allocated for each interrupt source. Therefore, four priority levels (0, 1, 2, and 3) are possible. The priority value is zero by default, and is also the highest priority.
  Note: The BLE subsystem is handled by ROM firmware and BLE-specific interrupts are with default priority value equal to zero (highest priority). It is only possible to set the same or lesser priority than BLE-specific for other peripheral interrupts. Same or lesser priority interrupts cannot interrupt the running ISR. The latency to serve other peripheral interrupt when BLE ISR is servicing depends on the full execution time for BLE ISR.
- Enable NVIC interrupt of specific IRQ numbers using ISER register.

Table 6-2. ATSAMB11 Interrupt Vector Table

IRQ Number	ISR Index	Interrupt Source	Muxability
-15	1	Reset	Non-muxable
-14	2	NMI	Non-muxable
-13	3	Hard Fault	Non-muxable
-5	11	SVC	Non-muxable
-2	14	Pending SV	Non-muxable
-1	15	SysTick	Non-muxable
0	16	UART0 RX	Muxable
1	17	UART0 TX	Muxable
2	18	UART1 RX	Muxable
3	19	UART1 TX	Muxable
4	20	SPI0 RX	Muxable
5	21	SPI0 TX	Muxable
6	22	SPI1 RX	Muxable
7	23	SPI1 TX	Muxable
8	24	I^2C0 RX	Muxable
9	25	I^2C0 TX	Muxable
10	26	I^2C1 RX	Muxable
11	27	I^2C1 TX	Muxable
12	28	Watchdog 0	Muxable(1)
13	29	Watchdog 1	Muxable
14	30	ARM® Dual Timer	Muxable
15	31	BLE Peripheral Register	Muxable
16	32	EFuse Out of Reset	Muxable(1)
17	33	BLE Security	Muxable(1)
18	34	SPI Flash	Muxable
19	35	Calibration Done	Muxable(1)
20	36	Brown Out Detected	Muxable
21	37	BLE specific	Non-Muxable(1)
22	38	BLE specific	Non-Muxable(1)
23	39	GPIO 0 Combined	Non-Muxable
24	40	GPIO 1 Combined	Non-Muxable

IRQ Number	ISR Index	Interrupt Source	Muxability
25	41	GPIO 2 combined	Non-Muxable
26	42	ARM timer	Non-Muxable(1)
27	43	AON sleep timer	Non-Muxable
28	44	BLE specific	Non-Muxable(1)
29	45	BLE specific	Non-Muxable(1)
30	46	BLE specific	Non-Muxable(1)
31	47	BLE specific	Non-Muxable(1)

Note:

1. This ISR index is used by the BLE stack. Applications must refrain from registering an ISR as it affects the chip functionality.

For more details on configuration options for muxable interrupts, see Muxable Interrupt.

7. Memory Subsystem

The Cortex-M0 core uses a 128 KB instruction/boot ROM along with a 128 KB shared instruction and data RAM.

7.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data used by the ARM. The 128 KB size of IDRAM1 and IDRAM2 is used for the BLE subsystem and also for the user application. IDRAM1 contains three 32 KB memories and IDRAM2 contains two 16 KB memories that are accessible to the ARM and used for instruction/data storage.

RAM memory is used by the user application as well as ROM firmware for data storage. The memory split-up between application and firmware might change when there is a BluSDK SMART release. Refer to BluSDK SMART Example Profiles Application User Guide for the memory map of this memory section.

7.2 ROM

The ROM is used to store the boot code and BLE firmware, stack, and selected user profiles. The ROM contains the 128 KB memory that is accessible to the ARM. The Boot loader code stored in ROM loads the application from Flash to RAM.

7.3 BLE Retention Memory

The BLE functionality requires 8 KB state, instruction, and data to be retained in memory, when the processor either goes into Sleep mode or Power down mode. The RAM is separated into specific power domains to allow tradeoff in power consumption with retention memory size.

7.4 Non-Volatile Memory

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This memory region is one-time- programmable. It is partitioned into six 128-bit banks. Each bank is divided into four blocks with each block containing 32 bits of memory locations. This non-volatile, one-time-programmable memory is used to store customer specific parameters as listed below.

- 26 MHz XO Calibration information
- BT address

The bit map for the block containing the above parameters is detailed in the following figures.

Figure 7-1. Bank 5 Block 0

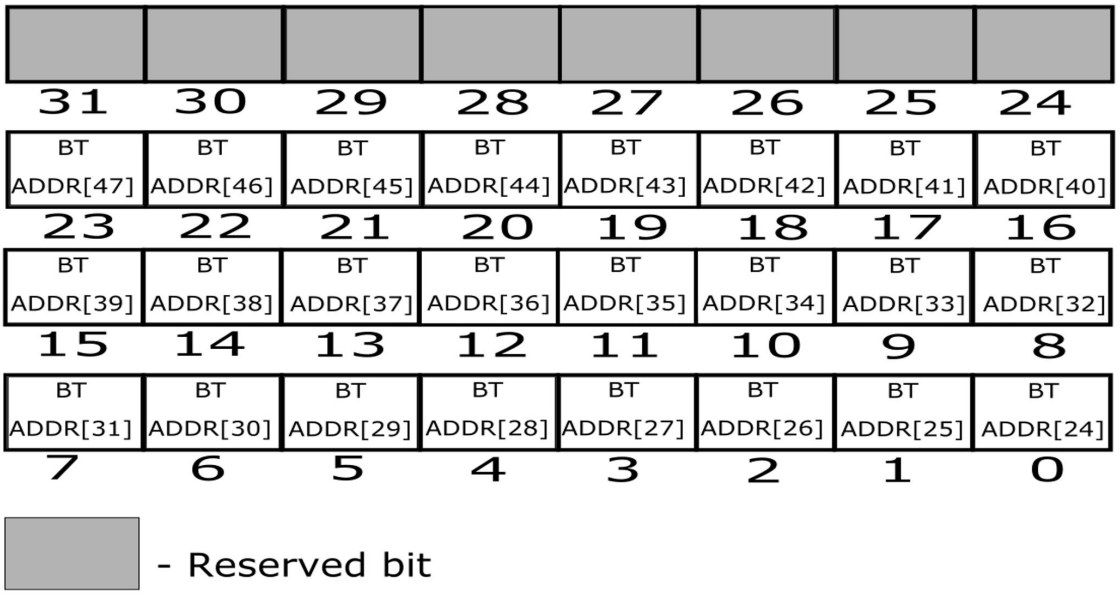


Figure 7-2. Bank 5 Block 1

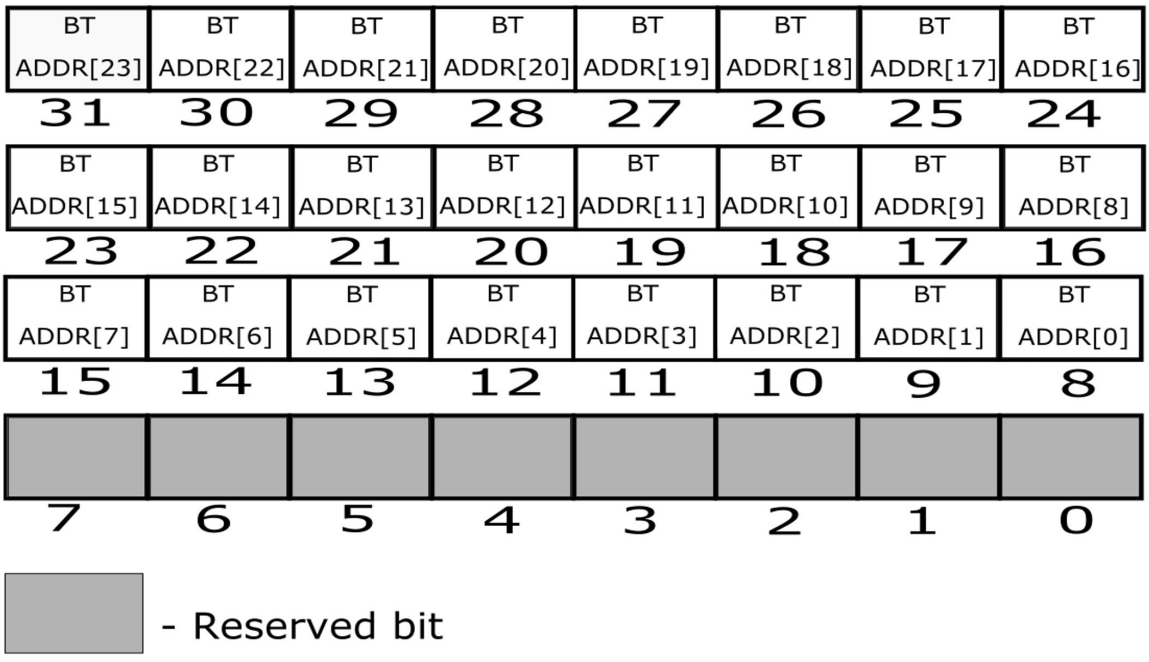
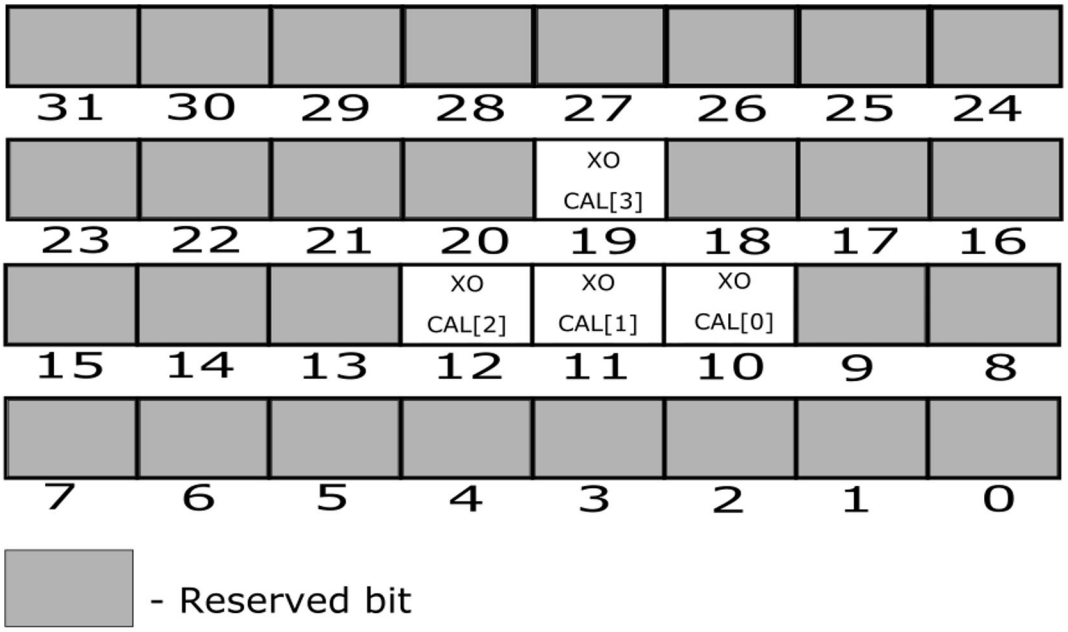


Figure 7-3. Bank 5 Block 3



The bits that are not depicted in the above register description are all reserved for future use.

7.4.1 26 MHz XO Calibration information

Information for both ATSAMB11-XR2100A and ATSAMB11-ZR210CA will be pre-programmed.

7.4.2 BT Address

These bits contain the BT address used by the user application. For ATSAMB11-ZR210CA modules, the BT address is pre-programmed. For ATSAMB11-XR2100A, the user must purchase the MAC address from IEEE and program it to the designated bit locations of the non-volatile memory.

7.4.3 Flash Memory

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have 256 kB of Flash memory, stacked on top of the MCU and BLE SoC. It is accessed through the SPI Flash controller.

Flash memory features are:

- 256 bytes per programmable page
- Uniform 4 kB Sectors, 32 kB & 64 kB Blocks
- Sector Erase (4 Kbyte)
- Block Erase (32 K or 64 Kbyte)
- Page program up to 256 bytes <1 ms
- More than 100,000 erase/write cycles and more than 20-year data retention
- 2.3 V to 3.6 V supply range

8. Bluetooth Low Energy Subsystem

The Bluetooth Low Energy (BLE) subsystem implements all the critical real-time functions required for full compliance with specification of the Bluetooth System v4.2, Bluetooth SIG. It consists of a Bluetooth 4.2 baseband controller (core), radio transceiver and the Microchip Bluetooth Smart Stack, and the BLE Software Platform.

8.1 BLE Core

The baseband controller consists of a modem and a Medium Access Controller (MAC) through which it encodes and decodes HCI packets. In addition, it constructs baseband data packages and schedules frames, and manages and monitors connection status, slot usage, data flow, routing, segmentation and buffer control.

The core performs Link Control Layer management supporting the main BLE states, including advertising and connection.

8.2 Features

- Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation, connect up to eight connections
- Frequency Hopping
- Advertising/Data/Control packet types
- Encryption (AES-128, SHA-256)
- Bitstream processing (CRC, whitening)
- Operating clock 52 MHz

8.3 BLE Radio

The radio consists of a fully integrated transceiver, low noise amplifier, Receive (RX) down converter, analog baseband processing, Phase Locked Loop (PLL), Transmit (TX) Power Amplifier, and Transmit/Receive switch. At the RF front end, no external RF components on the PCB are required other than the antenna and a matching component.

Table 8-1. ATSAMB11 BLE Radio features and properties

Feature	Description
Part Number	ATSAMB11-XR2100A and ATSAMB11-ZR210CA
BLE standard	Bluetooth V4.2 – Bluetooth Low Energy
Frequency range	2402 MHz to 2480 MHz
Number of channels	40
Modulation	GFSK
Data rate	1 Mbps

8.4 Microchip BluSDK Smart

The BluSDK Smart offers a comprehensive set of tools including reference applications for several Bluetooth SIG defined profiles and custom profile. This will help the user quickly evaluate, design and develop BLE products with ATSAMB11-XR2100A and ATSAMB11-ZR210CA.

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have a completely integrated Bluetooth Low Energy stack on chip that is fully qualified, mature, and Bluetooth V4.2 compliant.

Customer applications interface with the BLE protocol stack through the Microchip BLE API, which supports direct access to the GAP, SMP, ATT, GATT client / server, and L2CAP service layer protocols in the embedded firmware.

The stack includes numerous BLE profiles for applications like:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Automotive

Together with the Atmel Studio Software Development environment, the additional customer profiles can be easily developed.

In addition to the protocol stack, the drivers for each peripheral hardware block are provided as part of the Advanced Software Framework (ASF).

8.4.1 Direct Test Mode (DTM) Example Application

A DTM example application is among the reference applications offered in BluSDK Smart. Using this application, the user will be able to configure the device in the different test modes as defined in the Bluetooth Low Energy Core 4.2 specification (Vol6,Part F Direct Test Mode). Please refer the example getting started guide available in the BluSDK Smart release package.

9. Clocking

9.1 Overview

Figure 9-1. Clock Architecture

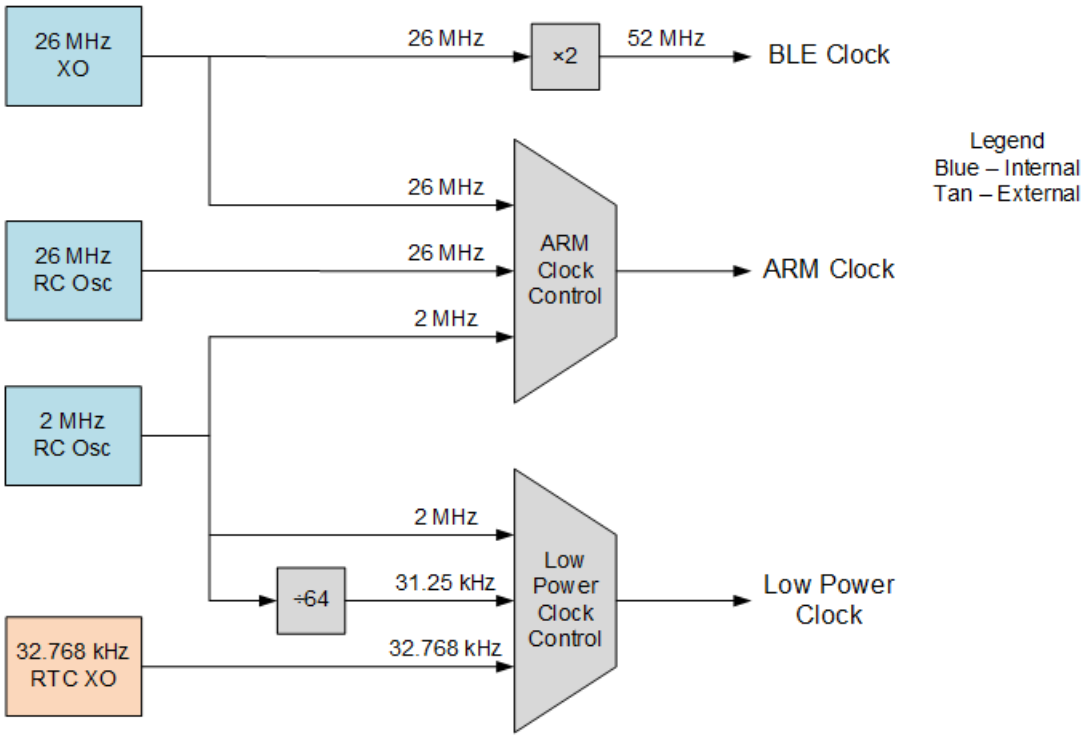


Figure 9-1 provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I^2C); the recommended MCU clock speed is 26 MHz. The Low Power Clock is used to drive all the low-power applications like the BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26 MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The frequency variation of 2 MHz integrated RC Oscillator is up to ±50% over process, voltage, and temperature.

The 32.768 kHz RTC Crystal Oscillator (RTC XO) is used for BLE operations as it will reduce power consumption by providing the best timing for wake-up precision, allowing circuits to be in low-power sleep mode for as long as possible until they need to wake-up and connect during the BLE connection event.

9.2 26 MHz Crystal Oscillator (XO)

A 26 MHz crystal oscillator is integrated into the ATSAMB11-XR2100A and ATSAMB11-ZR210CA to provide the precision clock for the BLE operations.

9.3 32.768 kHz RTC Crystal Oscillator (RTC XO)

9.3.1 General Information

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA contain a 32.768 kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500 ppm. Because of the high accuracy of the 32.768 kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power sleep mode for as long as possible, until they need to wake-up for the next connection timed event.

The block diagram in Figure 9-2 below shows how the internal low-frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15 pF on each terminal, RTC_CLK_P, and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, the user can program down the internal capacitance to its minimum value (~1 pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal, as illustrated in Figure 9-2 below.

The need for external bypass capacitors depends on the chosen crystal characteristics. Typically, the crystal should be chosen to have a load capacitance of 7 pF to minimize the oscillator current. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.

Alternatively, if an external 32.768 kHz clock is available, it can be used to drive the RTC_CLK_P pin instead of using a crystal. The XO has 6 pF internal capacitance on the RTC_CLK_P pin. To bypass the crystal oscillator, an external signal capable of driving 6 pF can be applied to the RTC_CLK_P terminal, as illustrated in Figure 9-2. RTC_CLK_N must be left unconnected, when driving an external source into RTC_CLK_P. Refer to the Table 9-1 for the specification of the external clock to be supplied at RTC_CLK_P.

Figure 9-2. Connections to RTC XO

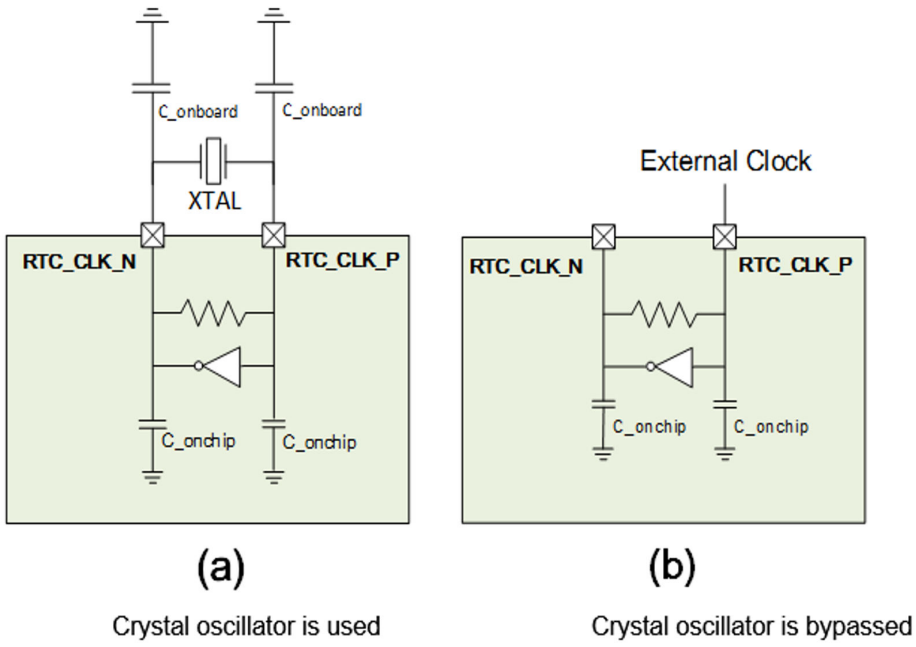


Table 9-1. 32.768 kHz External Clock Specification

Parameter	Min.	Typ.	Max	Unit	Comments
Oscillation frequency		32.768		kHz	Must be able to drive 6 pF load at desired frequency
VinH	0.7		1.2	V	High level input voltage
VinL	0		0.2		Low level input voltage
Stability – Temperature	-250		+250	ppm	

Additional internal trimming capacitors (C_onchip) are available. They provide the possibility to tune the frequency output of RTC XO without changing the external load capacitors. Contact technical support for usage of the internal trimming capacitors.

Note:
Refer the BluSDK BLE API Software Development Guide for details on how to enable the 32.768 kHz clock output and tune the internal trimming capacitors.

Table 9-2. 32.768 kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	C_onchip [pF]
0000	0.0
0001	1.0
0010	2.0
0011	3.0
0100	4.0
0101	5.0
0110	6.0
0111	7.0
1000	8.0
1001	9.0
1010	10.0
1011	11.0
1100	12.0
1101	13.0
1110	14.0
1111	15.0

9.3.2 RTC XO Design and Interface Specification

The RTC consists of two main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to guarantee start-up and to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with a supply voltage of 1.2V.

Table 9-3. RTC XO Interface

Pin Name	Function	Register Default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20 MOhm Feedback resistance 1 = 30 MOhm Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700 fF: 0000=700 fF 1111=11.2 pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt capacitance of 1.2 pF 1000= for crystal with shunt capacitance of >3 pF	0X4000F404<19:16>="1000"
VDD_XO	1.2V	

9.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp. = 25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at a supply voltage of 1.2V and temperature = 25°C.

Figure 9-3. RTC Drawn Current vs. Tuning Caps at 25°C

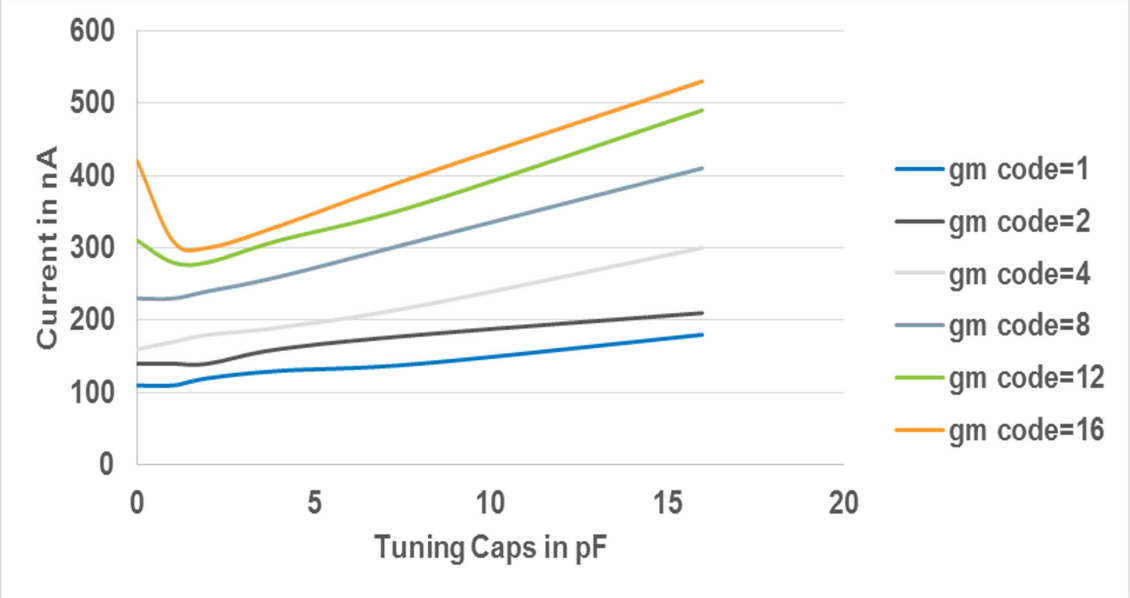
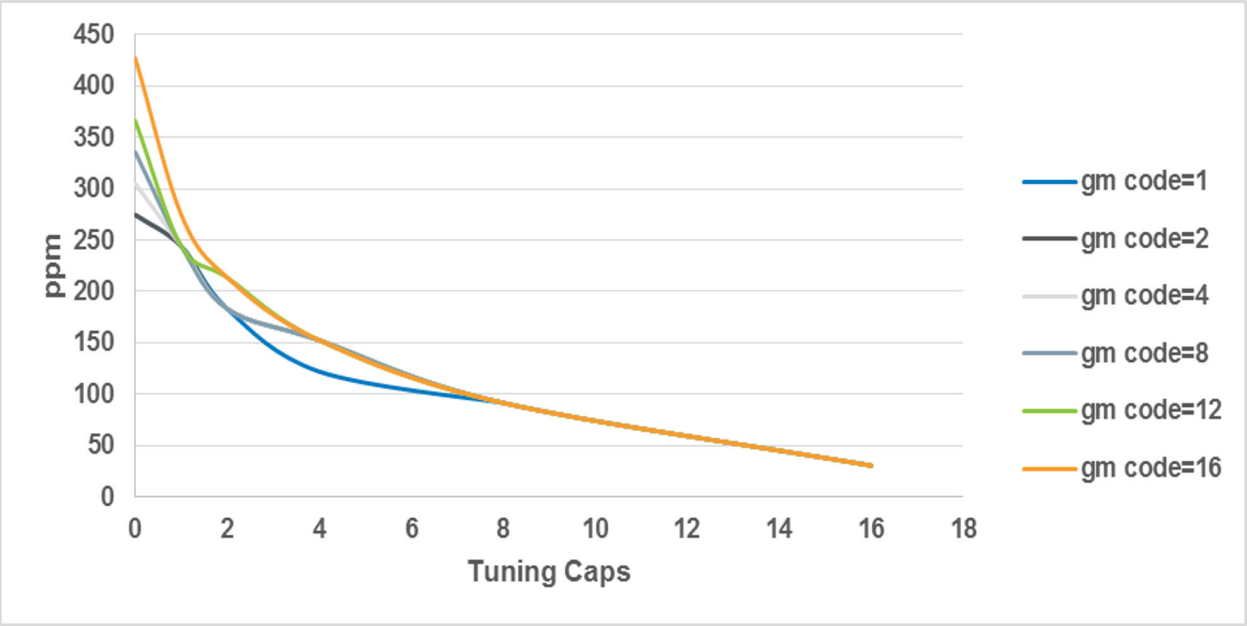


Figure 9-4. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



9.3.4 RTC Characterization with Supply Variation and Temp. = 25°C

Figure 9-5. RTC Drawn Current vs. Supply Variation

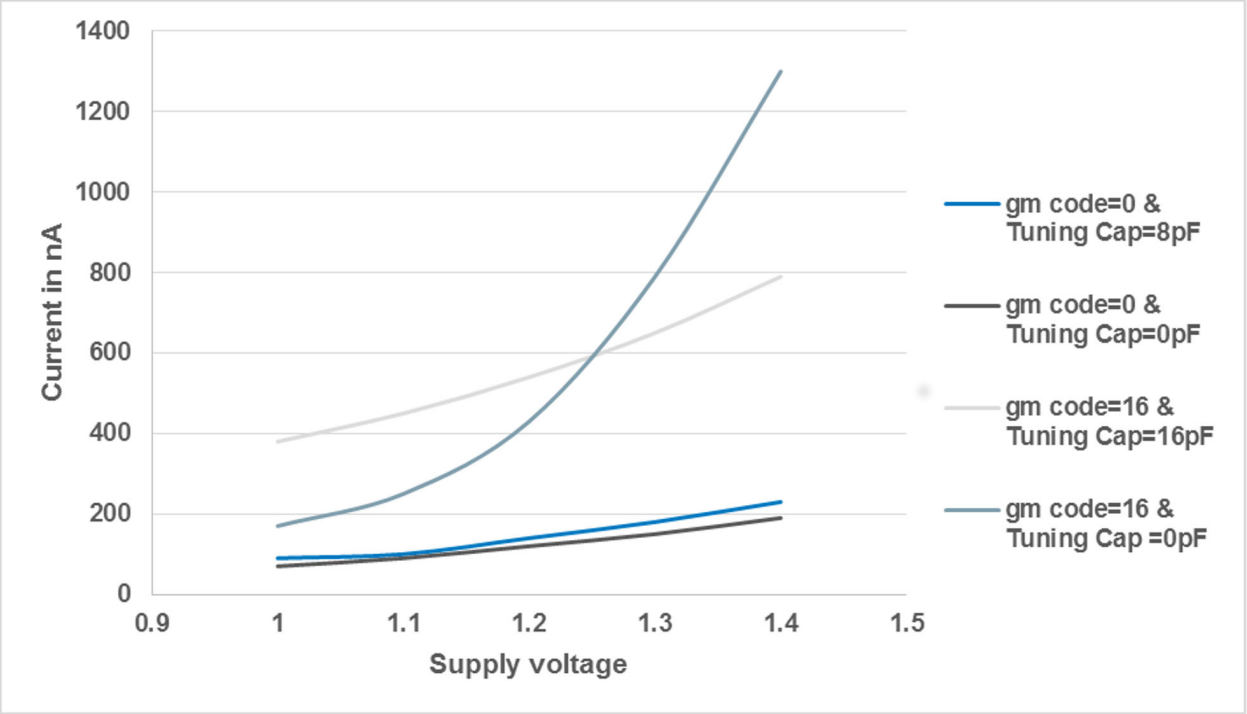
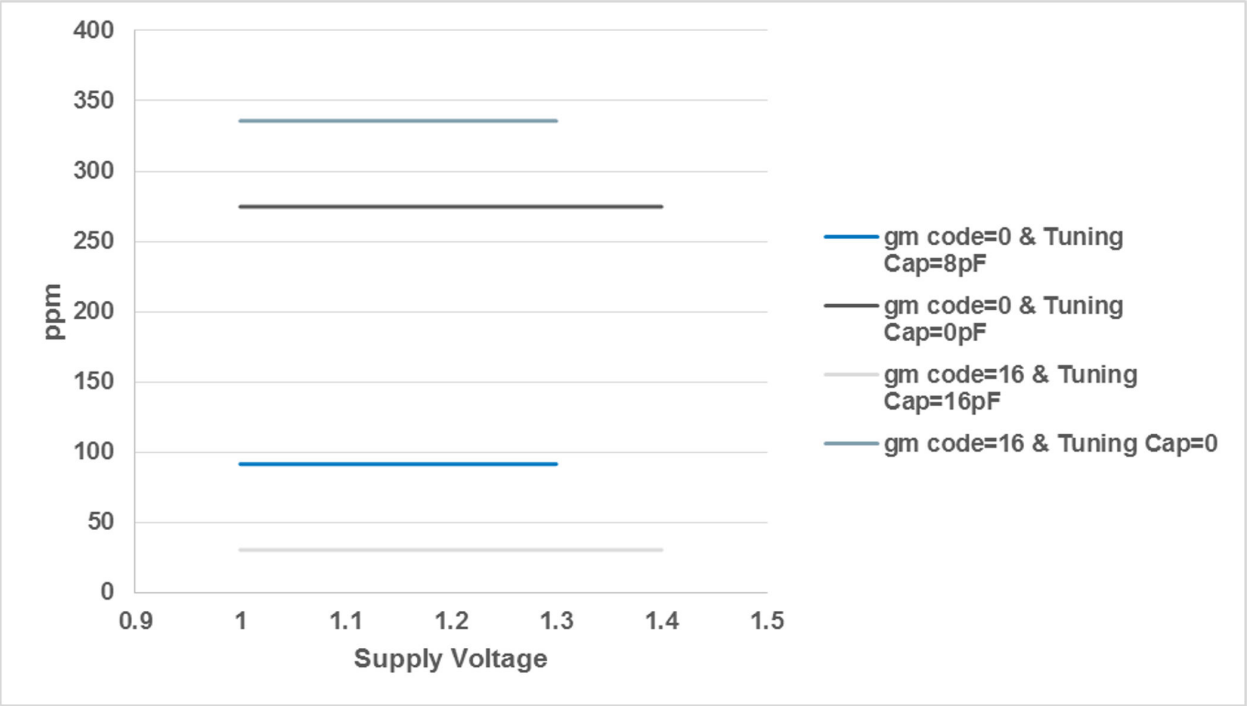


Figure 9-6. RTC Frequency Deviation vs. Supply Voltage



9.4 2 MHz Integrated RC Oscillator

The 2 MHz integrated RC Oscillator circuit without calibration contains a frequency variation of 50% over process, temperature, and voltage variation. As described above, calibration over process, temperature, and voltage is required to maintain the accuracy of this clock.

Figure 9-7. 32 kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

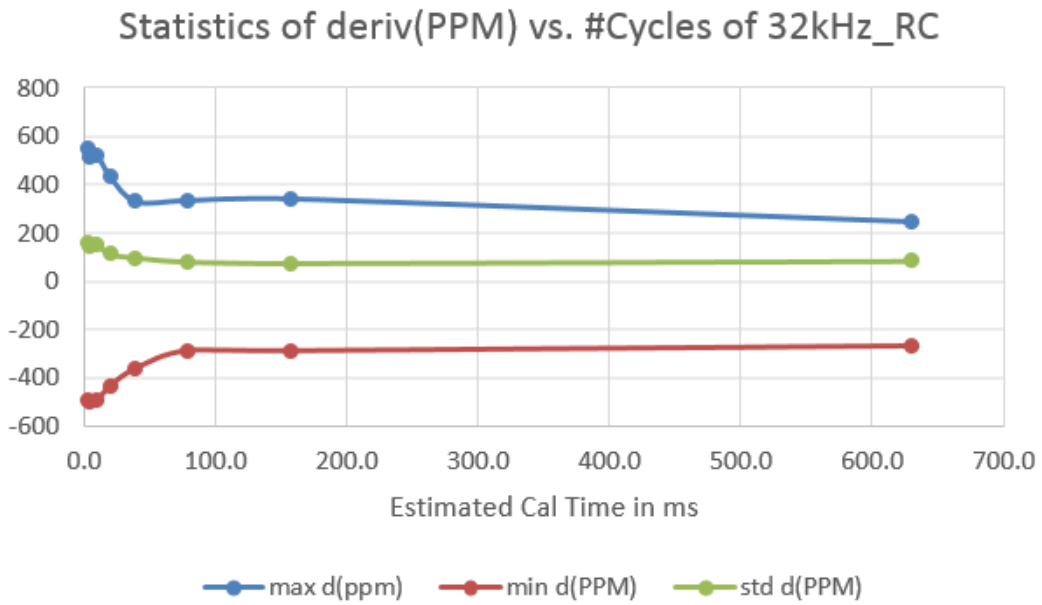
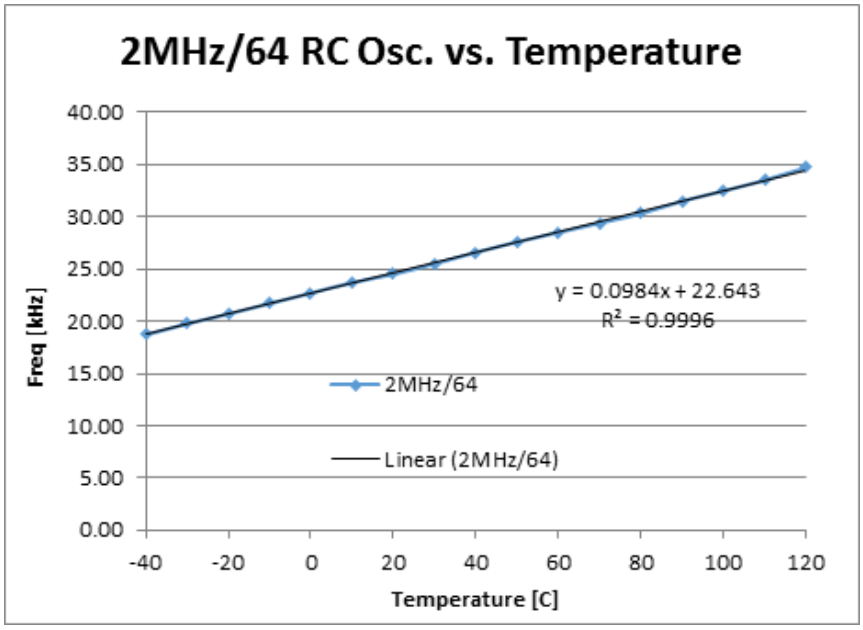


Figure 9-8. 32 kHz RC Oscillator Frequency Variation over Temperature



9.5 Clock Settings for Critical Sections

The three different clock sources 26 MHz XO, 26 MHz internal RC and 2 MHz internal RC can be used as input to ARM processor and other peripheral interfaces. As the clock configuration for some of the critical sections such as ARM, AON power sequencer, AON Sleep Timer, and BLE Sleep Timer are done by ROM firmware, the user is not recommended to change this clock configuration. This might affect the overall functionality. Therefore, the register descriptions related to this clock configurations are not provided.

9.5.1 ARM Processor Clock

26 MHz XO external crystal clock – this is the clock source for ARM processor and many of the peripherals.

9.5.2 AON Power Sequencer Clock

32.768 kHz RTC XO external crystal clock is the low power clock source for AON Power Sequencer module which controls the wake-up and sleep operations of ARM and BLE subsystem.

9.5.3 BLE Sleep Timer Clock

32.768 kHz RTC XO external crystal clock – this is the low power clock source for BLE Sleep Timer. This timer is used to wake-up BLE subsystem.

9.5.4 AON Sleep Timer Clock

32.768 kHz RTC XO external crystal clock – this is the low power clock source for AON Sleep Timer. This timer can be used by user application to wake-up ARM from ULP mode at predefined interval.

9.6 Peripheral Clock Configuration

ARM clock is the source for peripherals except for AON sleep timer. This clock is pre-scaled as per peripheral clock requirement. This clock is gated to peripherals and is enabled or disabled when required. This is to ensure the power is not consumed by the peripherals that are not used.

9.6.1 Enabling Peripheral Clock

Each peripheral clock is gated. Peripheral clock is enabled by setting the specific x_CLK_EN bit in LPMCU_CLOCK_ENABLES_0 or LPMCU_CLOCK_ENABLES_1 register. Few peripherals have gated clock for APB/AHB interface as well as for peripheral core operations. It is required to enable both the clocks for normal peripheral operation. For example, UART1_CORE_CLK_EN and UART1_IF_CLK_EN gate the clock for APB bus of UART1 and UART1 core operations.

Note: Few bits in these registers marked as “INTERNAL” are not recommended to change as those are controlled by ROM firmware.

9.6.2 Disabling Peripheral Clock

Peripheral clock is disabled by clearing the specific x_CLK_EN bit in LPMCU_CLOCK_ENABLES_0 or LPMCU_CLOCK_ENABLES_1 register.

9.6.3 Peripheral Reset

Each peripheral can be reset to default state by clearing the x_RSTN bit of LPMCU_GLOBAL_RESET_0 or LPMCU_GLOBAL_RESET_1 register. As long as x_RSTN bit is ‘0’ the peripheral is in reset state and cannot be configured for normal operations. Ensure that x_RSTN bit is set before configuring the peripheral for normal operation. The peripheral should be disabled before it is reset to avoid undefined behavior. Some peripherals have gated clock for APB/AHB interface as well as for peripheral core operations. It is required to reset both clock. For example, UART1_CORE_RSTN and UART1_IF_RSTN bits to be cleared for resetting APB bus and UART1 core.

Note: Some bits in these registers marked as “INTERNAL” are not recommended to change as those are controlled by ROM firmware.

9.7 AON Sleep Timer Clock Configuration

The 32.768 kHz RTC XO external crystal clock is given as clock source to AON Sleep Timer by ROM firmware. This clock is gated to enable or disable when required.

9.7.1 Enabling AON Sleep Timer Clock

The AON Sleep Timer clock is enabled by setting AON_SLEEP_TIMER_CLK_EN bit in AON_MISC_CTRL register.

Note: Some bits in these registers marked as “INTERNAL” are not recommended to change as those are controlled by ROM firmware.

9.7.2 Disabling AON Sleep Timer Clock

The AON Sleep Timer clock is disabled by clearing AON_SLEEP_TIMER_CLK_EN bit in AON_MISC_CTRL register.

9.7.3 AON Sleep Timer Reset

The AON Sleep Timer can be reset to default state by clearing the SLEEP_TIMER_RSTN bit of AON_GLOBAL_RESET register. As long as SLEEP_TIMER_RSTN bit is ‘0’ the AON Sleep Timer is in

reset state and cannot be configured for normal operations. Ensure that SLEEP_TIMER_RSTN bit is set before configuring the timer for normal operation. AON Sleep Timer should be disabled before it is reset in order to avoid undefined behavior.

Note: Some bits in these register marked as “INTERNAL” are not recommended to change as those are controlled by ROM firmware.

9.7.4 Global (Chip) Reset

By clearing the GLOBAL_RSTN bit of AON_GLOBAL_RESET register resets the entire chip. This is the auto set bit as it resets the entire chip.

9.8 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B004	LPMCU_MISC_REGS0	LPMCU_GLOBAL_RESET_0	7:0	SPI1_IF_RSTN	SPI1_CORE_RSTN	SPI0_IF_RSTN	SPI0_CORE_RSTN	SPI_FLASH0_RSTN	SPI_FLASH0_SYS_RSTN	CPU_RSTN	GLOBAL_RSTN
			15:8	UART1_IF_RSTN	UART1_CORE_RSTN	UART0_IF_RSTN	UART0_CORE_RSTN	TIMER0_RSTN	GPIO_RSTN	I2C0_IF_RSTN	I2C0_CORE_RSTN
			23:16	ARM_FREE_CLK_RSTN	DBUG_RSTN	CALIB_XBAR_IF_RSTN	CALIB_RSTN	MBIST_RSTN	IRQ_CTRLR_CORE_RSTN	WDT1_RSTN	WDT0_RSTN
			31:24	PWM3_RSTN	PWM2_RSTN	PWM1_RSTN	PWM0_RSTN	QUAD_DEC2_RSTN	QUAD_DEC1_RSTN	QUAD_DEC0_RSTN	ARM_PRESETN_RSTN
0x4000B008	LPMCU_MISC_REGS0	LPMCU_GLOBAL_RESET_1	7:0	SPI0_SCK_CLK_RSTN	SECURITY_AES_AHB_RSTN	SECURITY_AES_CORE_RSTN	SECURITY_SHA_AHB_RSTN	SECURITY_SHA_CORE_RSTN	I2C1_IF_RSTN	I2C1_CORE_RSTN	DUALTIMER0_RSTN
			15:8					PROV_DMA_CTRL0_RSTN	SPI1_SCK_PHASE_INT_CLK_RSTN	SPI0_SCK_PHASE_INT_CLK_RSTN	SPI1_SCK_CLK_RSTN
0x4000F010	AON_GP_REGS0	AON_GLOBAL_RESET	7:0				PD4_RSTN	BLE_LP_RSTN		SLEEP_TIMER_RSTN	GLOBAL_RSTN
0x4000B00C	LPMCU_MISC_REGS0	LPMCU_CLOCK_ENABLES_0	7:0	GPIO_CLK_EN		DUALTIMER0_CLK_EN	I2C0_CORE_CLK_EN	SPI1_CORE_CLK_EN	SPI0_CORE_CLK_EN	SPI_FLASH0_CLK_EN	
			15:8	UART1_CORE_CLK_EN	UART0_IF_CLK_EN	UART0_CORE_CLK_EN	WDT1_CLK_EN	WDT0_CLK_EN			TIMER0_CLK_EN
			23:16	ARM_PCLK_EN	AON_WRAPPER_CLK_EN	CALIB_XBAR_IF_CLK_EN	ROM_MEM_CLK_EN	IDRAM_2_GL_MEM_CLK_EN	IDRAM_1_GL_MEM_CLK_EN	IRQ_CTRLR_CORE_CLK_EN	UART1_IF_CLK_EN
			31:24		CALIB_CLK_EN	I2C1_CORE_CLK_EN	QUAD_DEC2_CLK_EN	QUAD_DEC1_CLK_EN	QUAD_DEC0_CLK_EN	BLE_MEM_CLK_EN	ARM_PCLKG_EN
0x4000B010	LPMCU_MISC_REGS0	LPMCU_CLOCK_ENABLES_1	7:0	PWM1_CLK_EN	PWM0_CLK_EN	EFUSE5_CLK_EN	EFUSE4_CLK_EN	EFUSE3_CLK_EN	EFUSE2_CLK_EN	EFUSE1_CLK_EN	EFUSE0_CLK_EN
			15:8	SHA_CORE_CLK_EN	TIMER0_PGCLK_EN	GPIO_GCLK_EN	SPI1_SCK_PHASE_INT_CLK_EN	SPI0_SCK_PHASE_INT_CLK_EN	SENS_ADC_CLK_EN	PWM3_CLK_EN	PWM2_CLK_EN
			23:16	IDRAM_2_1_MEM_CLK_EN	IDRAM_2_0_MEM_CLK_EN	IDRAM_1_2_MEM_CLK_EN	IDRAM_1_1_MEM_CLK_EN	IDRAM_1_0_MEM_CLK_EN	AES_AHB_CLK_EN	AES_CORE_CLK_EN	SHA_AHB_CLK_EN
0x4000F00C	AON_GP_REGS0	AON_MISC_CTRL	7:0		LPMCU_CPU_RESET_OVERRIDE_VAL	LPMCU_CPU_RESET_OVERRIDE_EN	LPMCU_USE_BOOT_REGS	LPMCU_BOOT_RESET_MUX_SEL	USE_EXT_32KHZ_CLK_SLEEP_TIMER	USE_RTC_32KHZ_CLK_SLEEP_TIMER	
			15:8	USE_OSC2M_AS_TB_CLK	USE_2M_AON_PWR_SEQ_CLK						
			23:16			FORCE_XO_TO_BYPASS_MODE	FORCE_OFF_XO	INVERT_WAKEUP_GPIO_0	USE_RTC_AON_PWR_SEQ_CLK	AON_EXT_32KHZ_OUT_EN	AON_SLEEP_TIMER_CLK_EN

9.9 Register Description

9.9.1 LPMCU Global Reset 0

Name: LPMCU_GLOBAL_RESET_0
Reset: 0xFFFFFFFD

Absolute Address: 0x4000B004

This register is a part of LPMCU_MISC_REGS0 Registers. This register allows the user to reset the individual peripherals.

Bit	31	30	29	28	27	26	25	24
	PWM3_RSTN	PWM2_RSTN	PWM1_RSTN	PWM0_RSTN	QUAD_DEC2_RSTN	QUAD_DEC1_RSTN	QUAD_DEC0_RSTN	ARM_PRESETN_RSTN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	ARM_FREE_CLK_RSTN	DBUG_RSTN	CALIB_XBAR_IF_RSTN	CALIB_RSTN	MBIST_RSTN	IRQ_CTRLR_CORE_RSTN	WDT1_RSTN	WDT0_RSTN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	UART1_IF_RSTN	UART1_CORE_RSTN	UART0_IF_RSTN	UART0_CORE_RSTN	TIMER0_RSTN	GPIO_RSTN	I2C0_IF_RSTN	I2C0_CORE_RSTN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	SPI1_IF_RSTN	SPI1_CORE_RSTN	SPI0_IF_RSTN	SPI0_CORE_RSTN	SPI_FLASH0_RSTN	SPI_FLASH0_SYS_RSTN	CPU_RSTN	GLOBAL_RSTN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	0	1

Bit 31 – PWM3_RSTN PWM3 Peripheral Reset
Writing '0' to this bit resets PWM3 peripheral
Writing '1' to this bit allows normal PWM3 peripheral operations

Bit 30 – PWM2_RSTN PWM2 Peripheral Reset
Writing '0' to this bit resets PWM2 peripheral
Writing '1' to this bit allows normal PWM2 peripheral operations

Bit 29 – PWM1_RSTN PWM1 Peripheral Reset
Writing '0' to this bit resets PWM1 peripheral
Writing '1' to this bit allows normal PWM1 peripheral operations

Bit 28 – PWM0_RSTN PWM0 Peripheral Reset
Writing '0' to this bit resets PWM0 peripheral
Writing '1' to this bit allows normal PWM0 peripheral operations

Bit 27 – QUAD_DEC2_RSTN Quad Decoder 2 Peripheral Reset
Writing '0' to this bit resets Quad Decoder 2 peripheral
Writing '1' to this bit allows normal Quad Decoder 2 peripheral operations

Bit 26 – QUAD_DEC1_RSTN Quad Decoder 1 Peripheral Reset
Writing '0' to this bit resets Quad Decoder 1 peripheral
Writing '1' to this bit allows normal Quad Decoder 1 peripheral operations

Bit 25 – QUAD_DEC0_RSTN Quad Decoder 0 Peripheral Reset
Writing '0' to this bit resets Quad Decoder 0 peripheral
Writing '1' to this bit allows normal Quad Decoder 0 peripheral operations

Bit 24 – ARM_PRESETN_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 23 – ARM_FREE_CLK_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 22 – DBUG_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 21 – CALIB_XBAR_IF_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 20 – CALIB_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 19 – MBIST_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 18 – IRQ_CTRLR_CORE_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 17 – WDT1_RSTN
Writing '0' to this bit resets Watchdog 1 peripheral
Writing '1' to this bit allows normal Watchdog 1 peripheral operations

Bit 16 – WDT0_RSTN
Writing '0' to this bit resets Watchdog 0 peripheral
Writing '1' to this bit allows normal Watchdog 0 peripheral operations

Bit 15 – UART1_IF_RSTN
Writing '0' to this bit resets UART1 peripheral interface
Writing '1' to this bit allows normal UART1 peripheral interface operations

Bit 14 – UART1_CORE_RSTN
Writing '0' to this bit resets APB operation of UART1 peripheral core
Writing '1' to this bit allows normal UART1 peripheral core APB operations

Bit 13 – UART0_IF_RSTN
Writing '0' to this bit resets UART0 peripheral interface
Writing '1' to this bit allows normal UART0 peripheral interface operations

Bit 12 – UART0_CORE_RSTN
Writing '0' to this bit resets APB operation of UART0 peripheral core
Writing '1' to this bit allows normal UART0 peripheral core APB operations

Bit 11 – TIMER0_RSTN
Writing '0' to this bit resets Timer 0 peripheral
Writing '1' to this bit allows normal Timer 0 peripheral operations

Bit 10 – GPIO_RSTN
Writing '0' to this bit resets GPIO Controllers
Writing '1' to this bit allows normal GPIO Controllers operations

Bit 9 – I2C0_IF_RSTN
Writing '0' to this bit resets I2C0 peripheral interface
Writing '1' to this bit allows normal I2C0 peripheral interface operations

Bit 8 – I2C0_CORE_RSTN
Writing '0' to this bit resets APB operation of I2C0 peripheral core
Writing '1' to this bit allows normal I2C0 peripheral core APB operations

Bit 7 – SPI1_IF_RSTN
Writing '0' to this bit resets SPI1 peripheral interface
Writing '1' to this bit allows normal SPI1 peripheral interface operations

Bit 6 – SPI1_CORE_RSTN
Writing '0' to this bit resets APB operation of SPI1 peripheral core
Writing '1' to this bit allows normal SPI1 peripheral core APB operations

Bit 5 – SPI0_IF_RSTN
Writing '0' to this bit resets SPI0 peripheral interface
Writing '1' to this bit allows normal SPI0 peripheral interface operations

Bit 4 – SPI0_CORE_RSTN
Writing '0' to this bit resets APB operation of SPI0 peripheral core
Writing '1' to this bit allows normal SPI0 peripheral core APB operations

Bit 3 – SPI_FLASH0_RSTN
Writing '0' to this bit resets SPI Flash peripheral interface
Writing '1' to this bit allows normal SPI Flash peripheral interface operations

Bit 2 – SPI_FLASH0_SYS_RSTN
Writing '0' to this bit resets AHB operation of SPI Flash peripheral system
Writing '1' to this bit allows normal SPI Flash peripheral core AHB operations

Bit 1 – CPU_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

Bit 0 – GLOBAL_RSTN
This is an 'INTERNAL' bit. Controlled by ROM firmware and not recommended to change

9.9.2 LPMCU Global Reset 1

Name: LPMCU_GLOBAL_RESET_1
Reset: 0xFFF

Absolute Address: 0x4000B008

This register is a part of LPMCU_MISC_REGS0 Registers. This register allows the user to reset the individual peripherals.

Bit	15	14	13	12	11	10	9	8
					PROV_DMA_CTRL0_RSTN	SPI1_SCK_PHASE_INT_CLK_RSTN	SPI0_SCK_PHASE_INT_CLK_RSTN	SPI1_SCK_CLK_RSTN
Access					R/W	R/W	R/W	R/W
Reset					1	1	1	1

Bit	7	6	5	4	3	2	1	0
	SPI0_SCK_CLK_RSTN	SECURITY_AES_AHB_RSTN	SECURITY_AES_CORE_RSTN	SECURITY_SHA_AHB_RSTN	SECURITY_SHA_CORE_RSTN	I2C1_IF_RSTN	I2C1_CORE_RSTN	DUALTIMER0_RSTN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 11 – PROV_DMA_CTRL0_RSTN
Writing '0' to this bit resets DMA Controller
Writing '1' to this bit allows normal DMA Controller operations

Bit 10 – SPI1_SCK_PHASE_INT_CLK_RSTN
Writing '0' to this bit resets logic that is on SPI1 SCK Phase int clock. Phase int clock is same clock as that of SPI Master SCK clock, that can get inverted depending on the phase setting for the SPI.
Writing '1' to this bit allows normal operations

Bit 9 – SPI0_SCK_PHASE_INT_CLK_RSTN
Writing '0' to this bit resets logic that is on SPI0 SCK Phase int clock. Phase int clock is same clock as that of SPI Master SCK clock, that can get inverted depending on the phase setting for the SPI.
Writing '1' to this bit allows normal operations

Bit 8 – SPI1_SCK_CLK_RSTN
Writing '0' to this bit resets logic that is on SPI1 Master clock
Writing '1' to this bit allows normal operations

Bit 7 – SPI0_SCK_CLK_RSTN
Writing '0' to this bit resets logic that is on SPI0 Master clock
Writing '1' to this bit allows normal operations

Bit 6 – SECURITY_AES_AHB_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 5 – SECURITY_AES_CORE_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 4 – SECURITY_SHA_AHB_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 3 – SECURITY_SHA_CORE_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 2 – I2C1_IF_RSTN
Writing '0' to this bit resets I2C1 peripheral interface
Writing '1' to this bit allows normal I2C1 peripheral interface operations

Bit 1 – I2C1_CORE_RSTN
Writing '0' to this bit resets I2C1 APB operations of peripheral core
Writing '1' to this bit allows normal I2C1 peripheral core APB operations

Bit 0 – DUALTIMER0_RSTN
Writing '0' to this bit resets Dual Timer peripheral
Writing '1' to this bit allows normal operations of Dual Timer

9.9.3 AON Global Reset

Name: AON_GLOBAL_RESET
Reset: 0x1B

Absolute Address: 0x4000F010

This register is a part of AON_GP_REGS0 Registers. This register allows the user to reset the individual Always-On power domain peripherals.

Bit	7	6	5	4	3	2	1	0
				PD4_RSTN	BLE_LP_RSTN		SLEEP_TIMER_RSTN	GLOBAL_RSTN
Access				R/W	R/W		R/W	R/W
Reset				1	1		1	1

Bit 4 – PD4_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 3 – BLE_LP_RSTN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 1 – SLEEP_TIMER_RSTN
Writing '0' to this bit resets AON Sleep Timer peripheral
Writing '1' to this bit allows normal AON Sleep Timer operations

Bit 0 – GLOBAL_RSTN
Writing '0' to this bit resets entire chip
This is an auto set bit, resets entire chip

9.9.4 LPMCU Clock Enable 0

Name: LPMCU_CLOCK_ENABLES_0
Reset: 0x 627FF9BE

Absolute Address: 0x4000B00C

This register is a part of LPMCU_MISC_REGS0 Registers. This register allows the user to enable clock for individual peripherals.

Bit	31	30	29	28	27	26	25	24
		CALIB_CLK_EN	I2C1_CORE_CLK_EN	QUAD_DEC2_CLK_EN	QUAD_DEC1_CLK_EN	QUAD_DEC0_CLK_EN	BLE_MEM_CLK_EN	ARM_PCLKG_EN
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	1	0	0	0	1	0

Bit	23	22	21	20	19	18	17	16
	ARM_PCLK_EN	AON_WRAPPER_CLK_EN	CALIB_XBAR_IF_CLK_EN	ROM_MEM_CLK_EN	IDRAM_2_GL_MEM_CLK_EN	IDRAM_1_GL_MEM_CLK_EN	IRQ_CTRLR_CORE_CLK_EN	UART1_IF_CLK_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	UART1_CORE_CLK_EN	UART0_IF_CLK_EN	UART0_CORE_CLK_EN	WDT1_CLK_EN	WDT0_CLK_EN			TIMER0_CLK_EN
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	1	1	1	1	1			1

Bit	7	6	5	4	3	2	1	0
	GPIO_CLK_EN		DUALTIMER0_CLK_EN	I2C0_CORE_CLK_EN	SPI1_CORE_CLK_EN	SPI0_CORE_CLK_EN	SPI_FLASH0_CLK_EN	
Access	R/W		R/W	R/W	R/W	R/W	R/W	
Reset	1		1	1	1	1	1	

Bit 30 – CALIB_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 29 – I2C1_CORE_CLK_EN
Writing '0' to this bit disables clock to I2C1 core APB interface
Writing '1' to this bit enables clock to I2C1 core APB interface

Bit 28 – QUAD_DEC2_CLK_EN
Writing '0' to this bit disables clock to Quad Decoder2
Writing '1' to this bit enables clock to Quad Decoder2

Bit 27 – QUAD_DEC1_CLK_EN
Writing '0' to this bit disables clock to Quad Decoder1
Writing '1' to this bit enables clock to Quad Decoder1

Bit 26 – QUAD_DEC0_CLK_EN
Writing '0' to this bit disables clock to Quad Decoder0
Writing '1' to this bit enables clock to Quad Decoder0

Bit 25 – BLE_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 24 – ARM_PCLKG_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 23 – ARM_PCLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 22 – AON_WRAPPER_CLK_EN
This is an INTERNAL bit and not recommended to change

Bit 21 – CALIB_XBAR_IF_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 20 – ROM_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 19 – IDRAM_2_GL_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 18 – IDRAM_1_GL_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 17 – IRQ_CTRLR_CORE_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 16 – UART1_IF_CLK_EN
Writing '0' to this bit disables clock to UART1 interface
Writing '1' to this bit enables clock to UART1 interface

Bit 15 – UART1_CORE_CLK_EN
Writing '0' to this bit disables clock to UART1 core APB interface
Writing '1' to this bit enables clock to UART1 core APB interface

Bit 14 – UART0_IF_CLK_EN
Writing '0' to this bit disables clock to UART0 interface
Writing '1' to this bit enables clock to UART0 interface

Bit 13 – UART0_CORE_CLK_EN
Writing '0' to this bit disables clock to UART0 core APB interface
Writing '1' to this bit enables clock to UART0 core APB interface

Bit 12 – WDT1_CLK_EN
Writing '0' to this bit disables clock to Watchdog Timer1
Writing '1' to this bit enables clock to Watchdog Timer1

Bit 11 – WDT0_CLK_EN
Writing '0' to this bit disables clock to Watchdog Timer0
Writing '1' to this bit enables clock to Watchdog Timer0

Bit 8 – TIMER0_CLK_EN
Writing '0' to this bit disables clock to Timer0
Writing '1' to this bit enables clock to Timer0

Bit 7 – GPIO_CLK_EN
Writing '0' to this bit disables clock to GPIO controllers
Writing '1' to this bit enables clock to GPIO controllers

Bit 5 – DUALTIMER0_CLK_EN
Writing '0' to this bit disables clock to Dual Timer
Writing '1' to this bit enables clock to Dual Timer

Bit 4 – I2C0_CORE_CLK_EN
Writing '0' to this bit disables clock to I2C0 core APB interface
Writing '1' to this bit enables clock to I2C0 core APB interface

Bit 3 – SPI1_CORE_CLK_EN
Writing '0' to this bit disables clock to SPI1 core APB interface
Writing '1' to this bit enables clock to SPI1 core APB interface

Bit 2 – SPI0_CORE_CLK_EN
Writing '0' to this bit disables clock to SPI0 core APB interface
Writing '1' to this bit enables clock to SPI0 core APB interface

Bit 1 – SPI_FLASH0_CLK_EN
Writing '0' to this bit disables clock to SPI Flash0
Writing '1' to this bit enables clock to SPI Flash0

9.9.5 LPMCU Clock Enable 1

Name: LPMCU_CLOCK_ENABLES_1
Reset: 0xF8783F

Absolute Address: 0x4000B010

This register is a part of LPMCU_MISC_REGS0 Registers. This register allows the user to enable clock for individual peripherals.

Bit	23	22	21	20	19	18	17	16
	IDRAM_2_1_MEM_CLK_EN	IDRAM_2_0_MEM_CLK_EN	IDRAM_1_2_MEM_CLK_EN	IDRAM_1_1_MEM_CLK_EN	IDRAM_1_0_MEM_CLK_EN	AES_AHB_CLK_EN	AES_CORE_CLK_EN	SHA_AHB_CLK_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	0	0	0

Bit	15	14	13	12	11	10	9	8
	SHA_CORE_CLK_EN	TIMER0_PGCLK_EN	GPIO_GCLK_EN	SPI1_SCK_PHASE_INT_CLK_EN	SPI0_SCK_PHASE_INT_CLK_EN	SENS_ADC_CLK_EN	PWM3_CLK_EN	PWM2_CLK_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	1	0	0	0

Bit	7	6	5	4	3	2	1	0
	PWM1_CLK_EN	PWM0_CLK_EN	EFUSE5_CLK_EN	EFUSE4_CLK_EN	EFUSE3_CLK_EN	EFUSE2_CLK_EN	EFUSE1_CLK_EN	EFUSE0_CLK_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	1	1

Bit 23 – IDRAM_2_1_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 22 – IDRAM_2_0_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 21 – IDRAM_1_2_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 20 – IDRAM_1_1_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 19 – IDRAM_1_0_MEM_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 18 – AES_AHB_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 17 – AES_CORE_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 16 – SHA_AHB_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 15 – SHA_CORE_CLK_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 14 – TIMER0_PGCLK_EN
Writing '0' to this bit disables clock to Timer0 APB interface
Writing '1' to this bit enables clock to Timer0 APB interface

Bit 13 – GPIO_GCLK_EN
Writing '0' to this bit disables clock to GPIO AHB interface
Writing '0' to this bit enables clock to GPIO AHB interface

Bit 12 – SPI1_SCK_PHASE_INT_CLK_EN
Writing '0' to this bit disables SPI1 SCK Phase int clock. Phase int clock is same clock as that of SPI Master SCK clock, that can get inverted depending on the phase setting for the SPI.
Writing '1' to this bit enables SPI1 SCK Phase int clock

Bit 11 – SPI0_SCK_PHASE_INT_CLK_EN
Writing '0' to this bit disables SPI0 SCK Phase int clock. Phase int clock is same clock as that of SPI Master SCK clock, that can get inverted depending on the phase setting for the SPI.
Writing '1' to this bit enables SPI0 SCK Phase int clock

Bit 10 – SENS_ADC_CLK_EN
Writing '0' to this bit disables ADC peripheral clock
Writing '1' to this bit enables ADC peripheral clock

Bit 9 – PWM3_CLK_EN
Writing '0' to this bit disables PWM3 peripheral clock
Writing '1' to this bit enables PWM3 peripheral clock

Bit 8 – PWM2_CLK_EN
Writing '0' to this bit disables PWM2 peripheral clock
Writing '1' to this bit enables PWM2 peripheral clock

Bit 7 – PWM1_CLK_EN
Writing '0' to this bit disables PWM1 peripheral clock
Writing '1' to this bit enables PWM1 peripheral clock

Bit 6 – PWM0_CLK_EN
Writing '0' to this bit disables PWM0 peripheral clock
Writing '1' to this bit enables PWM0 peripheral clock

Bit 5 – EFUSE5_CLK_EN
Writing '0' to this bit disables EFUSE Bank 6 clock
Writing '1' to this bit enables EFUSE Bank6 clock

Bit 4 – EFUSE4_CLK_EN
Writing '0' to this bit disables EFUSE Bank 5 clock

Writing '1' to this bit enables EFUSE Bank 5 clock

Bit 3 – EFUSE3_CLK_EN
Writing '0' to this bit disables EFUSE Bank 4 clock
Writing '1' to this bit enables EFUSE Bank 4 clock

Bit 2 – EFUSE2_CLK_EN
Writing '0' to this bit disables EFUSE Bank 3 clock
Writing '1' to this bit enables EFUSE Bank 3 clock

Bit 1 – EFUSE1_CLK_EN
Writing '0' to this bit disables EFUSE Bank 2 clock
Writing '1' to this bit enables EFUSE Bank 2 clock

Bit 0 – EFUSE0_CLK_EN
Writing '0' to this bit disables EFUSE Bank 1 clock
Writing '1' to this bit enables EFUSE Bank 1 clock

9.9.6 AON Clock Enable

Name: AON_MISC_CTRL
Reset: 0x010000

Absolute Address: 0x4000F00C

This register is a part of AON_GP_REGS0 Registers. This register allows the user to enable clock for AON power domain peripherals.

Bit	23	22	21	20	19	18	17	16
			FORCE_XO_TO_BYPASS_MODE	FORCE_OFF_XO	INVERT_WAKEUP_GPIO_0	USE_RTC_AON_PWR_SEQ_CLK	AON_EXT_32KHZ_OUT_EN	AON_SLEEP_TIMER_CLK_EN
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8
	USE_OSC2M_AS_TB_CLK	USE_2M_AON_PWR_SEQ_CLK						
Access	R/W	R/W						
Reset	0	0						

Bit	7	6	5	4	3	2	1	0
		LPMCU_CPU_RESET_OVERRIDE_VAL	LPMCU_CPU_RESET_OVERRIDE_EN	LPMCU_USE_BOOT_REGS	LPMCU_BOOT_RESET_MUX_SEL	USE_EXT_32KHZ_CLK_SLEEP_TIMER	USE_RTC_32KHZ_CLK_SLEEP_TIMER	
Access		R/W	R/W	R/W	R/W	R/W	R/W	
Reset		0	0	0	0	0	0	

Bit 21 – FORCE_XO_TO_BYPASS_MODE
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 20 – FORCE_OFF_XO
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 19 – INVERT_WAKEUP_GPIO_0
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 18 – USE_RTC_AON_PWR_SEQ_CLK
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 17 – AON_EXT_32KHZ_OUT_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 16 – AON_SLEEP_TIMER_CLK_EN
Writing '0' to this bit disables AON Sleep Timer peripheral clock
Writing '1' to this bit enables AON Sleep Timer peripheral clock

Bit 15 – USE_OSC2M_AS_TB_CLK
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 14 – USE_2M_AON_PWR_SEQ_CLK
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 6 – LPMCU_CPU_RESET_OVERRIDE_VAL
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 5 – LPMCU_CPU_RESET_OVERRIDE_EN
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 4 – LPMCU_USE_BOOT_REGS
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 3 – LPMCU_BOOT_RESET_MUX_SEL
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 2 – USE_EXT_32KHZ_CLK_SLEEP_TIMER
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

Bit 1 – USE_RTC_32KHZ_CLK_SLEEP_TIMER
This is an INTERNAL bit. Controlled by ROM firmware and not recommended to change

10. I/O Peripheral Multiplexing and MEGAMUXing

This chapter describes the peripheral multiplexing and MEGAMUXing options of the I/O pins.

10.1 I/O Multiplexing

By default, each pin is controlled by the GPIO controller as a general purpose I/O. Alternatively, it can be assigned to one of the peripheral functions. The I/O pins are categorized into three different groups called LP_GPIO_x (Low Power), AO_GPIO_z (Always ON) and GPIO_MSy (Mixed Signal). To enable a specific peripheral function on a LP_GPIO_x pin, the PINMUX_SEL_n, (n=0,1..4) register corresponding to that pin must be written with the specific MUX value. The specific functionality on AO_GPIO_z pin is selected by configuring MUX value in the AON_PINMUX_SEL register. Only, MUX0 is possible for GPIO_MSy to configure either as digital or analog I/O using the MS_GPIO_MODE register.

Table 10-1. I/O Port Function Multiplexing

Pin Name	XR Pin No.	ZR Pin No.	GPIO Controller	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_0	35	12	GPIO0_00	Up/ Down	GPIO 0	MEGAMUX 0	SWD CLK	-	-	-	-	TEST OUT 0
LP_GPIO_1	36	13	GPIO0_01	Up/ Down	GPIO 1	MEGAMUX 1	SWD I/O	-	-	-	-	TEST OUT 1
LP_GPIO_2	37	14	GPIO0_02	Up/ Down	GPIO 2	MEGAMUX 2	UART0 RXD	-	SPI1 SCK	SPI0 SCK	SPI FLASH0 SCK	TEST OUT 2
LP_GPIO_3	38	15	GPIO0_03	Up/ Down	GPIO 3	MEGAMUX 3	UART0 TXD	-	SPI1 MOSI	SPI0 MOSI	SPI FLASH0 TXD	TEST OUT 3
LP_GPIO_4	39	16	GPIO0_04	Up/ Down	GPIO 4	MEGAMUX 4	UART0 CTS	-	SPI1 SSN	SPI0 SSN	SPI FLASH0 SSN	TEST OUT 4
LP_GPIO_5	2	17	GPIO0_05	Up/ Down	GPIO 5	MEGAMUX 5	UART0 RTS		SPI1 MISO	SPI0 MISO	SPI FLASH0 RXD	TEST OUT 5
LP_GPIO_6	3	18	GPIO0_06	Up/ Down	GPIO 6	MEGAMUX 6	UART1 RXD	-	-	SPI0 SCK	SPI FLASH0 SCK	TEST OUT 6
LP_GPIO_7	4	19	GPIO0_07	Up/ Down	GPIO 7	MEGAMUX 7	UART1 TXD	-	-	SPI0 MOSI	SPI FLASH0 TXD	TEST OUT 7
LP_GPIO_8	5	20	GPIO0_08	Up/ Down	GPIO 8	MEGAMUX 8	I^2C0 SDA	-	-	SPI0 SSN	SPI FLASH0 SSN	TEST OUT 8
LP_GPIO_9	6	21	GPIO0_09	Up/ Down	GPIO 9	MEGAMUX 9	I^2C0 SCL	-	-	SPI0 MISO	SPI FLASH0 RXD	TEST OUT 9
LP_GPIO_10	7	22	GPIO0_10	Up/ Down	GPIO 10	MEGAMUX 10	SPI0 SCK	-	-	-	SPI FLASH0 SCK	TEST OUT 10
LP_GPIO_11	8	23	GPIO0_11	Up/ Down	GPIO 11	MEGAMUX 11	SPI0 MOSI	-	-	-	SPI FLASH0 TXD	TEST OUT 11

Pin Name	XR Pin No.	ZR Pin No.	GPIO Controller	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_12	9	24	GPIO0_12	Up/ Down	GPIO 12	MEGAMUX 12	SPI0 SSN	-	-	-	SPI FLASH0 SSN	TEST OUT 12
LP_GPIO_13	10	25	GPIO0_13	Up/ Down	GPIO 13	MEGAMUX 13	SPI0 MISO	-	-	-	SPI FLASH0 RXD	TEST OUT 13
LP_GPIO_14	23	4	GPIO0_14	Up/ Down	GPIO 14	MEGAMUX 14	UART1 CTS	-	I^2C1 SDA	-	-	TEST OUT 14
LP_GPIO_15	24	5	GPIO0_15	Up/ Down	GPIO 15	MEGAMUX 15	UART1 RTS	-	I^2C1 SCL	-	-	TEST OUT 15
LP_GPIO_16	25	6	GPIO1_00	Up/ Down	GPIO 16	MEGAMUX 16	SPI FLASH0 SCK	-	SPI1 SSN	SPI0 SCK	SPI FLASH0 SSN	TEST OUT 16
LP_GPIO_17	28	8	GPIO1_01	Up/ Down	GPIO 17	MEGAMUX 17	SPI FLASH0 TXD	-	SPI1 SCK	SPI0 MOSI	-	TEST OUT 17
LP_GPIO_18	29	9	GPIO1_02	Up/ Down	GPIO 18	MEGAMUX 18	SPI FLASH0 SSN	-	SPI1 MISO	SPI0 SSN	SPI FLASH0 RXD	TEST OUT 18
LP_GPIO_19	30	10	GPIO1_03	Up/ Down	GPIO 19	MEGAMUX 19	SPI FLASH0 RXD	-	SPI1 MOSI	SPI0 MISO	-	TEST OUT 19
LP_GPIO_22	40		GPIO1_06	Up/ Down	GPIO 22	MEGAMUX 22	-	-	-	-	-	-
LP_GPIO_23	1		GPIO1_07	Up/ Down	GPIO 23	MEGAMUX 23	-	-	-	-	-	-
LP_GPIO_24	25		GPIO1_08	Up/ Down	GPIO 24	MEGAMUX 24	-	-	-	-	-	-
AO_GPIO_0	20	1	GPIO1_15	Up	GPIO 31	WAKEUP	RTC CLK IN	32kHZ CLK OUT	-	-	-	-
AO_GPIO_1	21	2	GPIO1_14	Up	GPIO 30	WAKEUP	RTC CLK IN	32kHZ CLK OUT	-	-	-	-
AO_GPIO_2	22	3	GPIO1_13	Up	GPIO 29	WAKEUP	RTC CLK IN	32kHZ CLK OUT	-	-	-	-
GPIO_MS1(1)	12	17	GPIO2_15	Up/ Down	GPIO 47	-	-	-	-	-	-	-
GPIO_MS2 (1)	13	18	GPIO2_14	Up/ Down	GPIO 46	-	-	-	-	-	-	-
GPIO_MS3 (1)	15	31	GPIO2_13	Up/ Down	GPIO 45	-	-	-	-	-	-	-
GPIO_MS4 (1)	16	32	GPIO2_12	Up/ Down	GPIO 44	-	-	-	-	-	-	-

Note:

1. If analog is selected, then the digital is disabled.

2. MUX2 is the default MUX value for LP_GPIO_0 and LP_GPIO_1 to function as Single Wire Debug (SWD) interface. It is not recommended to use these pins for other peripheral functionality, as these pins are used for programming/debugging.

10.1.1 Example

An example to illustrate the available options for LP_GPIO_3 pin, depending on the PINMUX_SEL [2:0] LP_GPIO_3 value selected on [14:12] bits of PINMUX_SEL_0 register:

- MUX0 – the pin functions general purpose I/O and is controlled by the GPIO controller.
- MUX1 – any option from the Table 10-2 is selected using MEGA_MUX_IO_SEL_n (n=0,1,2..6) register. It can be a quad_dec, pwm, or any of the other functions listed in the Table 10-2.
- MUX2 – the pin functions as UART1 TXD. This is achieved with the MUX1 option via MEGAMUX, but the MUX2 option allows a shortcut for the recommended pinout.
- MUX3 – this option is not used and thus defaults to MUX0.
- MUX4 – the pin functions as SPI1 MOSI.
- MUX5 – the pin functions as SPI0 MOSI.
- MUX6 – the pin functions as SPI FLASH0 SCK.
- MUX7 – the pin functions as bit 3 of the test output bus, giving access to various debug signals.

10.2 MEGAMUXing

In addition to peripheral multiplexing, the MEGAMUXing option allows more flexibility for mapping desired interfaces on I/O pins. The MUX1 option in Table 10-1 allows for any MEGAMUX option from Table 10-2 to be assigned to an I/O pin. When PINMUX_SEL_n (n=0 to 4) is assigned with MUX1 then the MEGA_MUX_IO_SEL_n (n=0 to 6) register is used to configure MEGAMUX for LP_GPIO_x I/O pins. MEGAMUX configuration is not possible for GPIO_MSy and AO_GPIO_z I/O pins.

The use case of the MEGAMUX option is that when a specific peripheral functionality is not available on an intended LP_GPIO_x pin through MUX2 to MUX6 configurations, the MEGAMUX option allows that functionality.

Table 10-2. MEGAMUX Options

MUX_Sel	Function
0x00	UART0 RXD
0x01	UART0 TXD
0x02	UART0 CTS
0x03	UART0 RTS
0x04	UART1 RXD
0x05	UART1 TXD
0x06	UART1 CTS
0x07	UART1 RTS
0x08	I^2C0 SDA

MUX_Sel	Function
0x09	I^2C0 SCL
0x0A	I^2C1 SDA
0x0B	I^2C1 SCL
0x0C	PWM 0
0x0D	PWM 1
0x0E	PWM 2
0x0F	PWM 3
0x10	LP CLOCK OUT
0x11	Reserved
0x12	Reserved
0x13	Reserved
0x14	Reserved
0x15	Reserved
0x16	Reserved
0x17	Reserved
0x18	Reserved
0x19	Reserved
0x1A	Reserved
0x1B	Reserved
0x1C	Reserved
0x1D	QUAD DEC X IN A
0x1E	QUAD DEC X IN B
0x1F	QUAD DEC Y IN A
0x20	QUAD DEC Y IN B
0x21	QUAD DEC Z IN A
0x22	QUAD DEC Z IN B

10.2.1 Example

An example of peripheral assignment using these MEGAMUX options is as follows:

- I²C0 PINMUXed on LP_GPIO_10 and LP_GPIO_11 via
  - PINMUX_SEL_1 register PINMUX_SEL[2:0] LP_GPIO_10 = 1 PINMUX_SEL[2:0] LP_GPIO_11 = 1.
  - MEGA_MUX_IO_SEL_2 register MEGAMUX_SEL[5:0] LP_GPIO_10 = 0x08 and MEGAMUX_SEL[5:0] LP_GPIO_11 = 0x09.
- I²C1 PINMUXed on LP_GPIO_0 and LP_GPIO_1 via
  - PINMUX_SEL_0 register PINMUX_SEL[2:0] LP_GPIO_0 = 1 PINMUX_SEL[2:0] LP_GPIO_1 = 1.
  - MEGA_MUX_IO_SEL_1 register MEGAMUX_SEL[5:0] LP_GPIO_0 = 0x0A and MEGAMUX_SEL[5:0] LP_GPIO_1 = 0x0B.

10.3 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B044	LPMCU_MISC_REGS0	PINMUX_SEL_0	7:0		PINMUX_SEL[2:0] LP_GPIO_1				PINMUX_SEL[2:0] LP_GPIO_0		
			15:8		PINMUX_SEL[2:0] LP_GPIO_3				PINMUX_SEL[2:0] LP_GPIO_2		
			23:16		PINMUX_SEL[2:0] LP_GPIO_5				PINMUX_SEL[2:0] LP_GPIO_4		
			31:24		PINMUX_SEL[2:0] LP_GPIO_7				PINMUX_SEL[2:0] LP_GPIO_6		
0x4000B048	LPMCU_MISC_REGS0	PINMUX_SEL_1	7:0		PINMUX_SEL[2:0] LP_GPIO_9				PINMUX_SEL[2:0] LP_GPIO_8		
			15:8		PINMUX_SEL[2:0] LP_GPIO_11				PINMUX_SEL[2:0] LP_GPIO_10		
			23:16		PINMUX_SEL[2:0] LP_GPIO_13				PINMUX_SEL[2:0] LP_GPIO_12		
			31:24		PINMUX_SEL[2:0] LP_GPIO_15				PINMUX_SEL[2:0] LP_GPIO_14		
0x4000B04C	LPMCU_MISC_REGS0	PINMUX_SEL_2	7:0		PINMUX_SEL[2:0] LP_GPIO_17				PINMUX_SEL[2:0] LP_GPIO_16		
			15:8		PINMUX_SEL[2:0] LP_GPIO_19				PINMUX_SEL[2:0] LP_GPIO_18		
			23:16		PINMUX_SEL[2:0] LP_GPIO_21				PINMUX_SEL[2:0] LP_GPIO_20		
			31:24		PINMUX_SEL[2:0] LP_GPIO_23				PINMUX_SEL[2:0] LP_GPIO_22		
0x4000B080	LPMCU_MISC_REGS0	PINMUX_SEL_4	7:0						PINMUX_SEL[2:0] LP_GPIO_24		
			15:8								
			23:16								
			31:24								
0x4000B1A0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_0	7:0			MEGAMUX_SEL[5:0] LP_GPIO_0					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_1					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_2					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_3					
0x4000B1A4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_1	7:0			MEGAMUX_SEL[5:0] LP_GPIO_4					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_5					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_6					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_7					
0x4000B1A8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_2	7:0			MEGAMUX_SEL[5:0] LP_GPIO_8					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_9					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_10					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_11					
0x4000B1AC	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_3	7:0			MEGAMUX_SEL[5:0] LP_GPIO_12					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_13					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_14					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_15					

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B1B0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_4	7:0			MEGAMUX_SEL[5:0] LP_GPIO_16					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_17					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_18					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_19					
0x4000B1B4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_5	7:0			MEGAMUX_SEL[5:0] LP_GPIO_20					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_21					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_22					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_23					
0x4000B1B8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_6	7:0			MEGAMUX_SEL[5:0] LP_GPIO_24					
0x4000F000	AON_GP_REGS0	AON_PINMUX_SEL	7:0			PINMUX_SEL[1:0] AO_GPIO_1				PINMUX_SEL[1:0] AO_GPIO_0	
			15:8							PINMUX_SEL[1:0] AO_GPIO_2	
0x4000F410	AON_GP_REGS0	MS_GPIO_MODE	7:0				ANALOG_EN GPIO_MS3	ANALOG_EN GPIO_MS2	ANALOG_EN GPIO_MS1	ANALOG_EN GPIO_MS0	

10.4 Register Description

10.4.1 LP_GPIO_x Peripheral Multiplexing 0

Name: PINMUX_SEL_0
Reset: 0x00000022

Absolute Address: 0x4000B044

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_0, LP_GPIO_1, LP_GPIO_2, LP_GPIO_3, LP_GPIO_4, LP_GPIO_5, LP_GPIO_6, LP_GPIO_7 pins as listed in Table 10-1.

Bit	31	30	29	28	27	26	25	24
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	1	0		0	1	0

Bits 30:28, 26:24, 22:20, 18:16, 14:12, 10:8, 6:4, 2:0 – PINMUX_SEL[2:0] LP_GPIO_x (x = 7 to 0) Pin mux configuration
These bits select peripheral function for LP_GPIO_x (x = 7 to 0; Replace x=7 for 30:28 bits, ... x=0 for 2:1 bits)

PINMUX_SEL[2:0]	Description
0x0	MUX0 peripheral function is selected
0x1	MUX1 (MEGAMUX) peripheral function is selected
0x2	MUX2 peripheral function is selected
0x3	MUX3 peripheral function is selected
0x4	MUX4 peripheral function is selected
0x5	MUX5 peripheral function is selected
0x6	MUX6 peripheral function is selected
0x7	MUX7 peripheral function is selected

10.4.2 LP_GPIO_x Peripheral Multiplexing 1

Name: PINMUX_SEL_1
Reset: 0x00000033

Absolute Address: 0x4000B048

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_8, LP_GPIO_9, LP_GPIO_10, LP_GPIO_11, LP_GPIO_12, LP_GPIO_13, LP_GPIO_14, LP_GPIO_15 pins as listed in Table 10-1.

Bit	31	30	29	28	27	26	25	24
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	1	1		0	1	1

Bits 30:28, 26:24, 22:20, 18:16, 14:12, 10:8, 6:4, 2:0 – PINMUX_SEL[2:0] LP_GPIO_x (x = 15 to 8)
Pin mux configuration
These bits select peripheral function for LP_GPIO_x (x = 15 to 8; Replace x=15 for 30:28 bits, ... x=8 for 2:1 bits)

PINMUX_SEL[2:0]	Description
0x0	MUX0 peripheral function is selected
0x1	MUX1 (MEGAMUX) peripheral function is selected
0x2	MUX2 peripheral function is selected
0x3	MUX3 peripheral function is selected
0x4	MUX4 peripheral function is selected
0x5	MUX5 peripheral function is selected
0x6	MUX6 peripheral function is selected
0x7	MUX7 peripheral function is selected

10.4.3 LP_GPIO_x Peripheral Multiplexing 2

Name: PINMUX_SEL_2
Reset: 0x00000000

Absolute Address: 0x4000B04C

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_16, LP_GPIO_17, LP_GPIO_18, LP_GPIO_19, LP_GPIO_20, LP_GPIO_21, LP_GPIO_22, LP_GPIO_23 pins as listed in Table 10-1.

Bit	31	30	29	28	27	26	25	24
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		PINMUX_SEL[2:0] LP_GPIO_x				PINMUX_SEL[2:0] LP_GPIO_x		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bits 30:28, 26:24, 22:20, 18:16, 14:12, 10:8, 6:4, 2:0 – PINMUX_SEL[2:0] LP_GPIO_x (x = 23 to 16)
Pin mux configuration
These bits select peripheral function for LP_GPIO_x (x = 23 to 16; Replace x=23 for 30:28 bits, ... x=16 for 2:1 bits)

PINMUX_SEL[2:0]	Description
0x0	MUX0 peripheral function is selected
0x1	MUX1 (MEGAMUX) peripheral function is selected
0x2	MUX2 peripheral function is selected
0x3	MUX3 peripheral function is selected
0x4	MUX4 peripheral function is selected
0x5	MUX5 peripheral function is selected
0x6	MUX6 peripheral function is selected
0x7	MUX7 peripheral function is selected

10.4.4 LP_GPIO_x Peripheral Multiplexing 4

Name: PINMUX_SEL_4
Reset: 0x00000000

Absolute Address: 0x4000B080

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_24 pin as listed in Table 10-1.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						PINMUX_SEL[2:0] LP_GPIO_x		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – PINMUX_SEL[2:0] LP_GPIO_x (x = 24) Pin mux configuration
These bits select peripheral function for LP_GPIO_x (x = 24).

PINMUX_SEL[2:0]	Description
0x0	MUX0 peripheral function is selected
0x1	MUX1 (MEGAMUX) peripheral function is selected
0x2	MUX2 peripheral function is selected
0x3	MUX3 peripheral function is selected
0x4	MUX4 peripheral function is selected
0x5	MUX5 peripheral function is selected
0x6	MUX6 peripheral function is selected
0x7	MUX7 peripheral function is selected

10.4.5 LP_GPIO_x Mega Multiplexing 0

Name: MEGA_MUX_IO_SEL_0
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1A0

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_0, LP_GPIO_1, LP_GPIO_2, LP_GPIO_3 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 3 to 0; Replace x=3 for 29:24 bits, ... x=0 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.6 LP_GPIO_x Mega Multiplexing 1

Name: MEGA_MUX_IO_SEL_1
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1A4

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_4, LP_GPIO_5, LP_GPIO_6, LP_GPIO_7 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 7 to 4; Replace x=7 for 29:24 bits, ... x=4 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.7 LP_GPIO_x Mega Multiplexing 2

Name: MEGA_MUX_IO_SEL_2
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1A8

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_8, LP_GPIO_9, LP_GPIO_10, LP_GPIO_11 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 11 to 8; Replace x=11 for 29:24 bits, ... x=8 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.8 LP_GPIO_x Mega Multiplexing 3

Name: MEGA_MUX_IO_SEL_3
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1AC

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_12, LP_GPIO_13, LP_GPIO_14, LP_GPIO_15 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 15 to 12; Replace x=15 for 29:24 bits, ... x=12 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.9 LP_GPIO_x Mega Multiplexing 4

Name: MEGA_MUX_IO_SEL_4
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1B0

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_16, LP_GPIO_17, LP_GPIO_18, LP_GPIO_19 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 19 to 16; Replace x=19 for 29:24 bits, ... x=16 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.10 LP_GPIO_x Mega Multiplexing 5

Name: MEGA_MUX_IO_SEL_5
Reset: 0x3F3F3F3F

Absolute Address: 0x4000B1B4

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_20, LP_GPIO_21, LP_GPIO_22, LP_GPIO_23 pins using MEGAMUX configuration as listed in Table 10-2.

Bit	31	30	29	28	27	26	25	24
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 29:24, 21:16, 13:8, 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 23 to 20; Replace x=23 for 29:24 bits, ... x=20 for 5:0 bits) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.11 LP_GPIO_x Mega Multiplexing 6

Name: MEGA_MUX_IO_SEL_6
Reset: 3F

Absolute Address: 0x4000B1B8

This register is a part of LPMCU_MISC_REGS0 registers. This register allows the user to enable a specific peripheral function on LP_GPIO_24 pin using MEGAMUX configuration as listed in Table 10-2.

Bit	7	6	5	4	3	2	1	0
			MEGAMUX_SEL[5:0] LP_GPIO_x					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			1	1	1	1	1	1

Bits 5:0 – MEGAMUX_SEL[5:0] LP_GPIO_x (x = 24) MEGAMUX configuration
These bits select peripheral function for LP_GPIO_x when, corresponding PINMUX_SEL[2:0] value in PINMUX_SEL_n register is 1 (MUX1).

See Table 10-2 for different possible peripheral options for MEGAMUX_SEL[5:0].

10.4.12 AO_GPIO_z Peripheral Multiplexing

Name: AON_PINMUX_SEL
Reset: 0x0001

Absolute Address: 0x4000F000

This register is a part of AON_GP_REGS0 registers. This register allows the user to enable a specific peripheral function on AO_GPIO_z pins as listed in I/O Port Function Multiplexing table.

Bit	15	14	13	12	11	10	9	8
							PINMUX_SEL[1:0] AO_GPIO_z	
Access							R/W	R/W
Reset							0	0

Bit	7	6	5	4	3	2	1	0
			PINMUX_SEL[1:0] AO_GPIO_z				PINMUX_SEL[1:0] AO_GPIO_z	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	1

Bits 9:8, 5:4, 1:0 – PINMUX_SEL[1:0] AO_GPIO_z (z = 2 to 0; Replace z=2 for 9:8 bits , ... z=0 for 1:0 bits) Pin mux configuration
These bits select peripheral function for AO_GPIO_z pin.

PINMUX_SEL[1:0]	Description
0x0	MUX0 peripheral function is selected
0x1	MUX1 peripheral function is selected
0x2	MUX2 peripheral function is selected
0x3	MUX3 peripheral function is selected

10.4.13 GPIO_MSy Mixed Signal Mode Select

Name: MS_GPIO_MODE
Reset: 0x0F

Absolute Address: 0x4000F410

This register is a part of AON_GP_REGS0 registers. This register allows the user to configure GPIO_MSy as either digital I/O pin or analog input pin.

Bit	7	6	5	4	3	2	1	0
					ANALOG_EN GPIO_MSy	ANALOG_EN GPIO_MSy	ANALOG_EN GPIO_MSy	ANALOG_EN GPIO_MSy
Access					R/W	R/W	R/W	R/W
Reset					1	1	1	1

Bits 3,2,1,0 – ANALOG_EN GPIO_MSy (y = 1 to 4 ; y=1 for bit 3, ... y=4 for bit 0) Mixed Signal Mode Select
Writing '0' to a bit configures GPIO_MSy as digital I/O.

Writing '1' to a bit configures GPIO_MSy as an analog input pin.

11. Muxable Interrupt

The Nested Vectored Interrupt Controller (NVIC) supports 32 interrupt lines. Each of the 32 interrupt lines is connected to one peripheral instance, as shown in the ATSAMB11 Interrupt Vector Table table. It is possible to change this default interrupt mapping to a different peripheral through muxable interrupt configuration. IRQ number 0 to IRQ number 20 are muxable interrupts.

The following table provides the list of interrupt options available for each of the muxable interrupts. IRQ_MUX_IO_SEL_n (n = 0 to 20) is the register used to configure the muxable interrupt options. The default value of IRQ_MUX_IO_SEL_n is zero; that is, the IRQ source for the IRQ number (0 to 20) is default as mentioned in the ATSAMB11 Interrupt Vector Table.

The use case of the muxable interrupt option is that when a specific peripheral interrupt (eg: DMA Status) is not mapped in the default ATSAMB11 Interrupt Vector Table, then the peripheral interrupt can be mapped through the muxable interrupt configuration.

Table 11-1. ATSAMB11 Muxable Interrupt Options

Option	Interrupt Source
0x1	UART0 RX
0x2	UART0 TX
0x3	UART1 RX
0x4	UART1 TX
0x5	SPI0 RX
0x6	SPI0 TX
0x7	SPI1 RX
0x8	SPI1 TX
0x9	I^2C0 RX
0xA	I^2C0 TX
0xB	I^2C1 RX
0xC	I^2C1 TX
0xD	WDT0 – RESERVED
0xE	WDT1
0xF	ARM DUALTIMER
0x10	DMA STATUS
0x11	SECURITY
0x12	RESERVED
0x13	QUAD DECODER
0x14	RESERVED
0x15	RESERVED

Option	Interrupt Source
0x16	RESERVED
0x17	RESERVED
0x18	BROWNOUT DETECTED

11.1 Example

An example of providing interrupt source as QUAD DECODER for IRQ number 11 using the muxable interrupt options is as follows:

1. Configure IRQ_MUX_IO_SEL_2 register MUX_11[4:0] = 0x13.
2. Follow the steps provided in Functional Description for enabling the interrupt.

11.2 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B0C0	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_0	7:0				MUX_0[4:0]				
			15:8				MUX_1[4:0]				
			23:16				MUX_2[4:0]				
			31:24				MUX_3[4:0]				
0x4000B0C4	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_1	7:0				MUX_4[4:0]				
			15:8				MUX_5[4:0]				
			23:16				MUX_6[4:0]				
			31:24				MUX_7[4:0]				
0x4000B0C8	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_2	7:0				MUX_8[4:0]				
			15:8				MUX_9[4:0]				
			23:16				MUX_10[4:0]				
			31:24				MUX_11[4:0]				
0x4000B0CC	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_3	7:0				MUX_12[4:0]				
			15:8				MUX_13[4:0]				
			23:16				MUX_14[4:0]				
			31:24				MUX_15[4:0]				
0x4000B0D0	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_4	7:0				MUX_16[4:0]				
			15:8				MUX_17[4:0]				
			23:16				MUX_18[4:0]				
			31:24				MUX_19[4:0]				
0x4000B0D4	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_5	7:0				MUX_20[4:0]				

11.3 Register Description

11.3.1 IRQ Multiplexing 0

Name: IRQ_MUX_IO_SEL_0
Reset: 0x00000000

Absolute Address: 0x4000B0C0

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 0, IRQ number 1, IRQ number 2, IRQ number 3 as listed in the ATSAMB11 Interrupt Vector table.

Bit	31	30	29	28	27	26	25	24
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24, 20:16, 12:8, 4:0 – MUX_n[4:0] IRQ number (n) = 3 to 0 (n=3 for 28:24 bits and n=0 for 4:0 bits), IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

11.3.2 IRQ Multiplexing 1

Name: IRQ_MUX_IO_SEL_1
Reset: 0x00000000

Absolute Address: 0x4000B0C4

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 4, IRQ number 5, IRQ number 6, IRQ number 7 as listed in ATSAMB11 Interrupt Vector table.

Bit	31	30	29	28	27	26	25	24
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24, 20:16, 12:8, 4:0 – MUX_n[4:0] IRQ number (n) = 7 to 4 (n=7 for 28:24 bits and n=4 for 4:0 bits, IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

11.3.3 IRQ Multiplexing 2

Name: IRQ_MUX_IO_SEL_2
Reset: 0x00000000

Absolute Address: 0x4000B0C8

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 8, IRQ number 9, IRQ number 10, IRQ number 11 as listed in the ATSAMB11 Interrupt Vector table.

Bit	31	30	29	28	27	26	25	24
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24, 20:16, 12:8, 4:0 – MUX_n[4:0] IRQ number (n) = 11 to 8 (n=11 for 28:24 bits and n=8 for 4:0 bits, IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

11.3.4 IRQ Multiplexing 3

Name: IRQ_MUX_IO_SEL_3
Reset: 0x00000000

Absolute Address: 0x4000B0CC

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 12, IRQ number 13, IRQ number 14, IRQ number 15 as listed in the ATSAMB11 Interrupt Vector table.

Bit	31	30	29	28	27	26	25	24
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24, 20:16, 12:8, 4:0 – MUX_n[4:0] IRQ number (n) = 15 to 12 (n=15 for 28:24 bits and n=12 for 4:0 bits, IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

11.3.5 IRQ Multiplexing 4

Name: IRQ_MUX_IO_SEL_4
Reset: 0x00000000

Absolute Address: 0x4000B0D0

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 16, IRQ number 17, IRQ number 18, IRQ number 19 as listed in the ATSAMB11 Interrupt Vector table.

Bit	31	30	29	28	27	26	25	24
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 28:24, 20:16, 12:8, 4:0 – MUX_n[4:0] IRQ number (n) = 19 to 16 (n=19 for 28:24 bits and n=16 for 4:0 bits, IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

11.3.6 IRQ Multiplexing 5

Name: IRQ_MUX_IO_SEL_5
Reset: 0x00000000

Absolute Address: 0x4000B0D4

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to select the interrupt source for IRQ number 20 as listed in the ATSAMB11 Interrupt Vector table.

Bit	7	6	5	4	3	2	1	0
				MUX_n[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bits 4:0 – MUX_n[4:0] IRQ number (n) = 20, IRQ mux configuration
These bits select interrupt source for specific IRQ number.
Refer to the ATSAMB11 Muxable Interrupt Options table for different possible interrupt source options for MUX_n[4:0].

12. GPIO Pin Controller

The GPIO pin controller controls the I/O pins of the device. The I/O pins are organized in a series of groups, collectively referred to as a Port group. Each Port group can have up to 16 pins that can be configured and controlled individually or as a group. There are three Port groups on a SAMB11-XR/ZR device, controlled by three GPIO pin controllers. Each pin is either used for general-purpose I/O under direct application control or assigned to an embedded device peripheral. When used for general-purpose I/O, each pin is configured as input or output, with configurable pull-up/pull-down settings.

All I/O pins have true read-modify-write functionality when used for general purpose I/O. The direction or the output value of one or more pins may be changed explicitly without unintentionally changing the state of any other pins in the same port group by a single, atomic 16-bit write.

The GPIO controller is connected to the high-speed bus matrix through the AHB bus.

12.1 Features

The AHB GPIO controller provides a 16-bit I/O interface with the following properties:

- Selectable input and output configuration for each individual pin.
- Software-controlled multiplexing of peripheral functions on I/O pins.
- Configurable pull settings:
  - Internal pull-up or pull-down.
- Programmable interrupt generation capability:
  - Interrupt generation masking.
  - Edge-triggered on rising, falling.
  - Level-sensitive on high or low values.
- Thread safe operation by providing separate set and clear addresses for control registers.
- Inputs are sampled using a double flip-flop to avoid metastability issues.

12.2 Signal Description

The following table describes the signal description of the GPIO pins.

Table 12-1. Signal Description for GPIO Pins

Pin Name	Type	Description
LP_GPIO_x	Digital I/O	General-purpose I/O pin x
AO_GPIO_z	Digital I/O	General-purpose I/O pin z. It can also be used to wake-up the core from the Ultra-Low Power mode
GPIO_MSy	Mixed signal I/O	General-purpose I/O pin y. Analog input can be connected

12.3 I/O Lines

The I/O lines are mapped to pins of the physical device. The I/O lines are categorized based on different functionalities into three groups called LP_GPIO_x, AO_GPIO_z, GPIO_MSy, as shown in Table 12-1. However, all these GPIO's are controlled by one of three GPIO controllers.

The I/O lines are divided into three groups with each group of 16 pins controlled by an individual GPIO controller. Referring to the GPIO Controller column of Table 10-1, the I/O lines from GPIO0_00 to GPIO0_15 are controlled using GPIO0 controller; GPIO1_00 to GPIO1_15 are controlled using GPIO1 controller, and GPIO2_00 to GPIO2_15 are controlled using GPIO2 controller.

Each pin can be controlled by pinmux settings, which allow the pad to route internally to a dedicated peripheral function. When set to specific PINMUX value in PINMUX_SEL_n/AON_PINMUX_SEL_n, the selected peripheral controls the output state of the pad, and reads the current physical pad state.

For more details see, I/O Multiplexing.

12.4 Clock Configuration

The GPIO controller must be provided with clock source before configuring for normal operation. Two bits GPIO_CLK_EN, and GPIO_GCLK_EN enable the clock for GPIO controllers and its AHB interface. Both the bits must be set for GPIO controller normal operation. For more details on configuration, see Peripheral Clock Configuration.

12.5 Functional Description of LP_GPIO_x I/O Pins

The overview and peripheral multiplexing of LP_GPIO_x I/O pins are shown in the following figures.

Figure 12-1. Overview of LP_GPIO_x Port

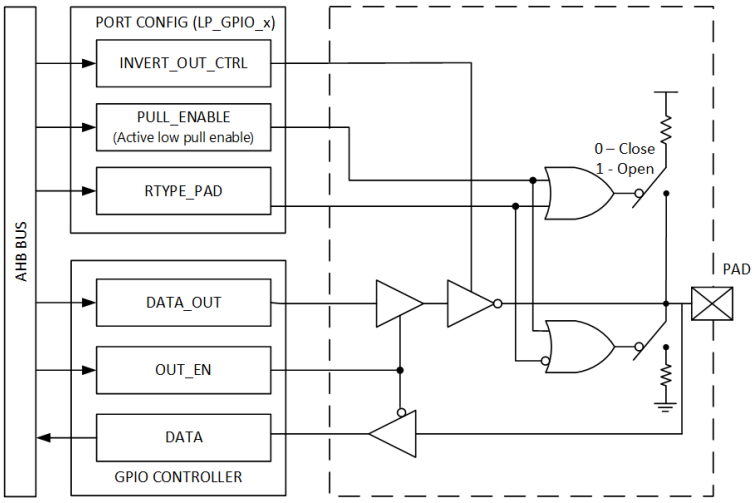
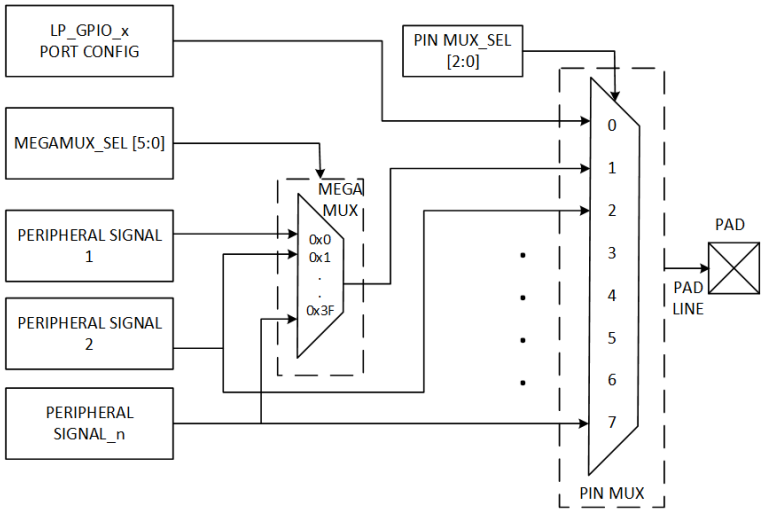


Figure 12-2. Overview of Peripheral Multiplexing for LP_GPIO_x Port



12.5.1 Initialization

After reset, all LP_GPIO_x pads are enabled with input and pull up. For more details, see the I/O Pin Behavior in the Different Device States table.

However, specific pins, such as those used for connection to a debugger are configured using PINMUX_SEL_n, as required by its special function.

12.5.2 Operation

1. Each LP_GPIO_x can be configured by the registers in PORT Config as shown in Figure 12-1. It is required to map a specific pin (LP_GPIO_x) to the GPIO controller which controls it. To control pin LP_GPIO_x, get the corresponding GPIO pin number ‘n’ and the GPIO controller number ‘p’ which controls it from I/O Multiplexing under GPIO Controller column (GPIOp_n).
   For example, LP_GPIO_18 is mapped to GPIO1_02. Here ‘p’ equals to 1, ‘n’ equals to 02 and ‘x’ equals to 18. In the configuration steps below, ‘n’ and ‘p’ are used to configure GPIO controller specific registers, and ‘x’ is used to configure LPMCU_MISC_REGS0 specific registers. 'n', 'p', 'x' value of specific LP_GPIO_x pin to be noted to configure that pin as general purpose I/O.
2. Configure PINMUX_SEL[2:0] bits of PINMUX_SEL_n register corresponding to x pin with MUX value equals to zero. Three bits are used to configure MUX for LP_GPIO_x pin.
   For example, to configure LP_GPIO_18: PINMUX_SEL_2 register PINMUX_SEL[2:0] LP_GPIO_18 = 0.
3. To use LP_GPIO_x pin as an output, write n bit of OUTENSET register of ‘p’ GPIO controller to '1'. The n bit in the DATAOUT register must be written to the desired output value. The output on pin ‘n’ can be inverted by configuring INVERT_OUT_CTRL register. To invert ‘n’ pin write ‘1’ of LP_GPIO_x bit on INVERT_OUT_CTRL register.
   For example, to configure LP_GPIO_18 as output: assign bit 2 of OUTENSET register of GPIO1(p) Controller to '1'.
4. To use pin LP_GPIO_x as an input, bit ‘n’ in the OUTENCLR register of ‘p’ GPIO controller must be written to '1'. The input value can be read from bit ‘n’ in register DATA.
   For example, to configure LP_GPIO_18 as input: assign bit 2 of OUTENCLR register of GPIO1(p) Controller to '1'.

The (PINMUX_SEL_n) registers select the peripheral function for the corresponding pin. When PINMUX_SEL[2:0] value is other than zero, then this overrides the connection between the GPIO

controller and the I/O pin, and connects the selected peripheral signal to the particular I/O pin instead of the GPIO Controller. For more information on different MUX configurations, see I/O Multiplexing.

12.5.3 I/O Pin Pull Configuration

The PULL_ENABLE and RTYPE_PAD registers are used to configure pull up or pull down on the LP_GPIO_x I/O pins as shown in the following pull configuration table. The internal pull up or pull down is mainly used for input; if the input pin is not connected, then Hi-z occurs. Enabling pull up or pull down leads to defined state on input line. The pull up or pull down circuit is common for input and output.

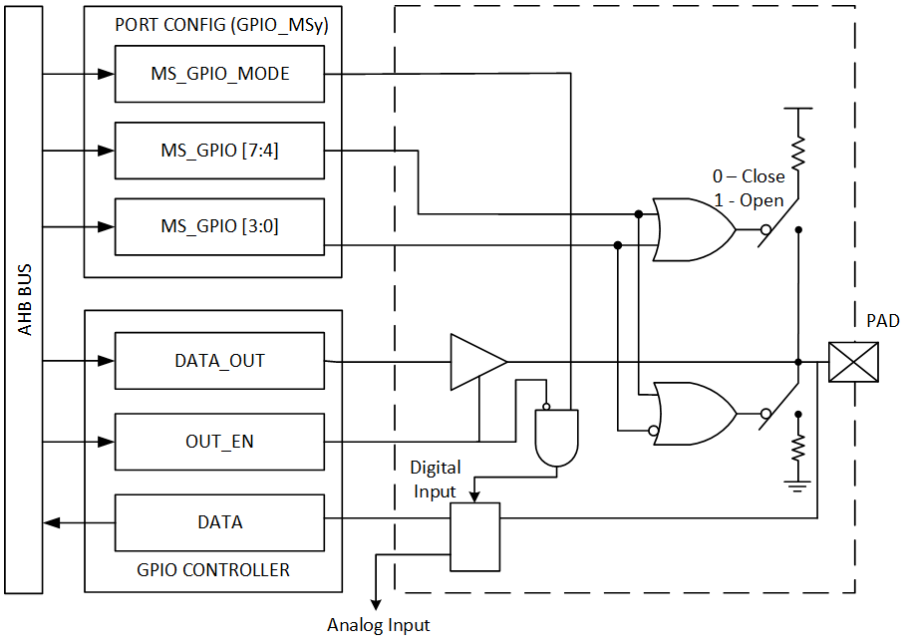
Table 12-2. Pull Configuration

OUTENSET	PULL_ENABLE	RTYPE_PAD	Configuration
0	0	0	Input with pull up
0	0	1	Input with pull down
0	1	0	Input; pull disabled If input line is floating then the value on pad is Hi-z. This means the sampled value in DATA register can be 0 or 1, and not a fixed value.
0	1	1	
1	0	0	Output with pull up
1	0	1	Output with pull down
1	1	0	Output; pull disabled
1	1	1	Output; pull disabled

12.6 Functional Description of GPIO_MSy I/O Pins

The overview of GPIO_MSy I/O pins is shown in the following figure.

Figure 12-3. Overview of GPIO_MSy Port



12.6.1 Initialization

After reset, all GPIO_MSy pads are configured as analog input pin with pull disabled.

12.6.2 Operation

The GPIO_MSy pins are mixed signal pins which are configured as analog or digital. Each GPIO_MSy can be configured by the registers in PORT Config as shown in Figure 12-3.

The GPIO_MSy pins are configured either as analog input pins or general purpose digital I/O pins using register MS_GPIO_MODE. By default, the GPIO_MSy pins are analog input pins with the MS_GPIO_MODE bit set for individual pins.

1. To use GPIO_MSy as general purpose I/O pin, clear the ANALOG_EN GPIO_MSy bit of MS_GPIO_MODE register.
2. Similar to LP_GPIO_x, it is required to get the corresponding GPIO_MSy pin number ‘n’ from I/O multiplexing under GPIO controller column. The GPIO_MSy I/O pins are controlled by GPIO2 controller. To use ‘n’ pin as an output, write ‘n’ bit of OUTENSET register of GPIO2 controller. The ‘n’ bit in the DATAOUT register must be written to the desired output value.
   For example, to configure GPIO_MS1 as output: assign bit 15 of OUTENSET register of GPIO2 Controller to '1'.
3. To use pin GPIO_MSy as an input, bit ‘n’ in the OUTENCLR register of GPIO2 Controller must be written to '1'. The input value can be read from bit ‘n’ in register DATA.
   For example, to configure GPIO_MS1 as input: assign bit 15 of OUTENCLR register of GPIO2 Controller to '1'.

12.6.3 I/O Pin Pull Configuration

The MS_GPIO register is used to configure pull up or pull down on the GPIO_MSy I/O pins as shown in the following pull configuration table. The pull up/down circuit is common for input and output.

Table 12-3. Pull Configuration

OUTENSET	MS_GPIO[7:4]	MS_GPIO[3:0]	Configuration
0	0	0	Input with pull up
0	0	1	Input with pull down
0	1	0	Input; pull disabled If input line is floating then the value on PAD is Hi-z. This means the value be sampled in DATA register can be 0 or 1, not a fixed value.
0	1	1	
1	0	0	Output with pull up
1	0	1	Output with pull down
1	1	0	Output; pull disabled
1	1	1	Output; pull disabled

12.7 Functional Description of AO_GPIO_z I/O Pins

The overview and peripheral multiplexing of AO_GPIO_z I/O pins are shown in the following figures.

Figure 12-4. Overview of AO_GPIO_z Port

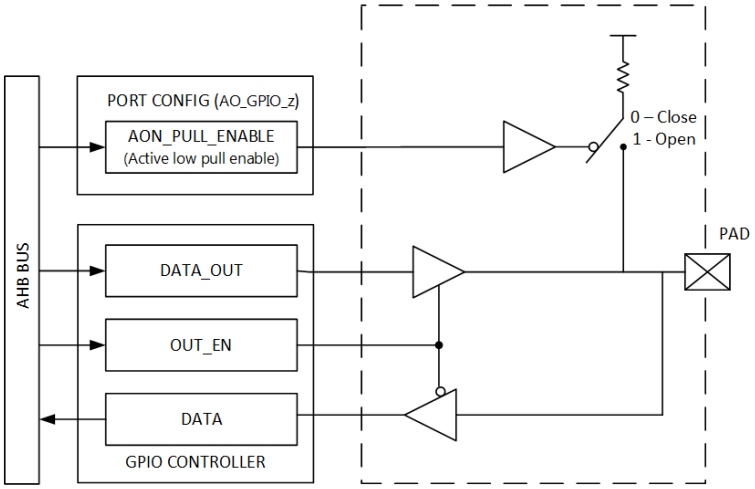
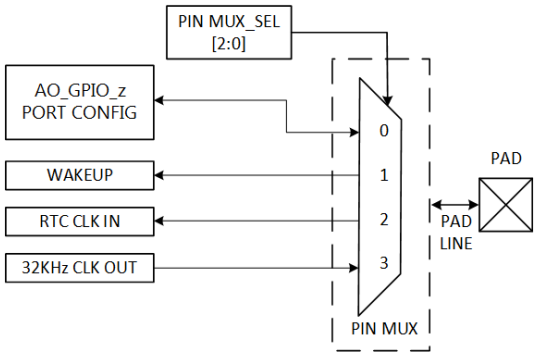


Figure 12-5. Overview of Peripheral Multiplexing for AO_GPIO_z Port



12.7.1 Initialization

After reset, all AO_GPIO_z pads are enabled with input and pull up. By default, the AO_GPIO_0 pin is configured to wake-up the core from the Ultra-Low Power (ULP) mode.

12.7.2 Operation

The AO_GPIO_z pins are special function I/O pins that are configured as general purpose I/O and also configured to wake-up (Wake-up Source) the core from the ULP mode.

1. To use AO_GPIO_z pin as an general-purpose I/O, configure PINMUX_SEL[1:0] of AON_PINMUX_SEL register corresponding to AO_GPIO_y pin with MUX value equals to zero. Two bits are used to configure MUX for AO_GPIO_z GPIO pin.
   For example, to configure AO_GPIO_1: AON_PINMUX_SEL register PINMUX_SEL[1:0] AO_GPIO_1 = 0.
2. Similar to LP_GPIO_x, it is required to get the corresponding AO_GPIO_z pin number ‘n’ from I/O Multiplexing under GPIO controller column. The AO_GPIO_z I/O lines are controlled by GPIO1 controller. To use AO_GPIO_z ‘n’ pin as an output, write n bit of OUTENSET register of GPIO1 controller. The n bit in the DATAOUT register must be written to the desired output value.
   For example, to configure AO_GPIO_1 as output: assign bit 30 of OUTENSET register of GPIO1 Controller to '1'.
3. To use pin AO_GPIO_z ‘n’ as an input, bit ‘n’ in the OUTENCLR register of GPIO1 controller must be written to '1'. The input value can be read from bit ‘n’ in register DATA.

For example, to configure AO_GPIO_1 as output: assign bit 30 of OUTENSET register of GPIO1 Controller to '1'.

The AON_PINMUX_SEL register selects the peripheral function for the corresponding AO_GPIO_z pin. When PINMUX_SEL[1:0] value is other than zero, then this overrides the connection between the GPIO controller and the I/O pin, and connects the selected peripheral signal to the particular I/O pin instead of the GPIO controller. For more information on different MUX configuration, see I/O Multiplexing.

12.7.3 I/O Pin Pull Configuration

The AON_PULL_ENABLE register is used to configure pull up on the AO_GPIO_z I/O pins as shown in the following pull configuration table. The pull up circuit is common for input and output.

Table 12-4. Pull Configuration

OUTENSET	AON_PULL_ENABLE	Configuration
0	0	Input with pull up
0	1	Input; pull disabled If input line is floating then the value on pad is Hi-z. This means the sampled value in DATA register can be 0 or 1, and not a fixed value.
1	0	Output with pull up
1	1	Output; pull disabled

12.7.4 Wake-up Source

The AO_GPIO_z pin can also wake-up the ARM Subsystem and BLE Subsystem from the ULP mode. Along with wake-up configuration, enabling an external interrupt generates an interrupt request. On reset, the AO_GPIO_0 as wake-up source is enabled by default.

1. To use AO_GPIO_z as wake-up source:
   - Wake-up source for ARM subsystem – configure AON_PINMUX_SEL with MUX1 and set the value as one for specific AO_GPIO_z pin.
   - Wake-up source for BLE subsystem – set the BLE_ENABLE bit on GPIO_WAKEUP_CTRL register. This configuration is common for all AO_GPIO_z pins.

     Note:
     - It is recommended to enable wake-up of ARM subsystem and BLE subsystem together. Enabling only the wake-up of BLE subsystem should not be performed.
     - Only AO_GPIO_0 can be configured as wake-up source with the present firmware. The AO_GPIO_1 and AO_GPIO_2 cannot be used as wake-up source at present.
     - As the firmware on ROM handles the wake-up and sleep operation, it is restricted to configure the AO_GPIO_z as rising interrupt only. Rising edge on AO_GPIO_z wakes-up the ARM and falling edge triggers the sleep. On rising edge, interrupt ROM firmware configures the AO_GPIO_z as falling edge. Until AO_GPIO_z is held high, the device is awake and awaits for falling edge on this pin. At falling edge, it triggers the interrupt and ROM firmware, configures the pin as rising edge, and enables sleep operation.
2. Configure AO_GPIO_z pin as input with external interrupt enable. For more details, see External Interrupt section.

12.8 External Interrupt

The GPIO Controller allows all GPIO pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z) to be configured as interrupt lines. Each interrupt line can be individually masked and can generate an interrupt to CPU on rising, falling, or on high or low levels.

12.8.1 Initialization

After reset, the interrupt is disabled on all GPIO pins.

12.8.2 Operation

To configure a GPIO pin as external interrupt, get the corresponding GPIO pin number ‘n’ and GPIO controller number ‘p’ from I/O Multiplexing table under the GPIO Controller column and perform the following initialization steps:

- Configure PINMUX_SEL_n or MS_GPIO_MODE or AON_PINMUX_SEL based in GPIO group with MUX0. When AO_GPIO_z is configured as wake-up source, then configure AON_PINMUX_SEL with MUX1.
- Initialize the GPIO pin direction as input. For LP_GPIO_x pin operation, GPIO_MSy pin operation and AO_GPIO_z pin operation, see Operation section.
- Refer to default pull configuration of the intended GPIO pin group and enable or disable pull based on the requirement.
- The GPIO controller provides programmable interrupt generation features. As shown in the following table, three registers control the operation, and each register has separate set and clear addresses. To configure each bit of the I/O pin (‘n’ bit on ‘p’ GPIO register) generate interrupt based on these three registers.

Table 12-5. Interrupt Configuration

Interrupt Enable Set (INTENSET)	Interrupt Polarity Set (INTPOLSET)	Interrupt Type Set (INTTYPESET)	Interrupt Feature
0	X	X	Disabled
1	0	0	Low-Level
1	0	1	Falling Edge
1	1	0	High-Level
1	1	1	Rising Edge

Note: External interrupts are double synchronized to FCLK(Free-running clock) before being converted to edge/level types and then is registered on FCLK. Hence, there are only three FCLK cycles latency on these interrupts for all of the four types (high level/low level/ rise edge/ fall edge) of interrupt configurations before being sensed by the processor.

- The interrupt request line is connected to the Interrupt Controller (NVIC). To use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. For more details, see Nested Vector Interrupt Controller.
- After an interrupt request is triggered, the corresponding bit in the INTSTATUSCLEAR register is set. The interrupt status can be cleared by writing 1 to the corresponding bit of the INTSTATUSCLEAR register.

12.9 Power Management

If the system goes to Ultra-Low Power mode, the GPIO controller is shut down and the latches in the pad retain their current configuration in the Sleep mode, such as the output value and pull settings. However, the PORT configuration registers lose their content, and these cannot be restored when PORT is powered-up again. Therefore, user must reconfigure the PORT peripheral at power-up to ensure it is in a well-defined state before use. For more details on reconfiguration, refer to the ATSAMB11 BluSDK Smart Interrupts and ULP Architecture and Usage User guide. This document also explains on how sleep and wake-up are controlled.

12.10 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x40010000 (GPIO0), 0x40011000 (GPIO1), 0x40013000 (GPIO2)	GPIO Controller	DATA	7:0	DATA[7:0]							
			15:8	DATA[15:8]							
0x40010004 (GPIO0), 0x40011004 (GPIO1), 0x40013004 (GPIO2)	GPIO Controller	DATAOUT	7:0	DATAOUT[7:0]							
			15:8	DATAOUT[15:8]							
0x40010010 (GPIO0), 0x40011010 (GPIO1), 0x40013010 (GPIO2)	GPIO Controller	OUTENSET	7:0	OUTENSET[7:0]							
			15:8	OUTENSET[15:8]							
0x40010014 (GPIO0), 0x40011014 (GPIO1), 0x40013014 (GPIO2)	GPIO Controller	OUTENCLR	7:0	OUTENCLR[7:0]							
			15:8	OUTENCLR[15:8]							
0x40010020 (GPIO0), 0x40011020 (GPIO1), 0x40013020 (GPIO2)	GPIO Controller	INTENSET	7:0	INTENSET[7:0]							
			15:8	INTENSET[15:8]							
0x40010024 (GPIO0), 0x40011024 (GPIO1), 0x40013024 (GPIO2)	GPIO Controller	INTENCLR	7:0	INTENCLR[7:0]							
			15:8	INTENCLR[15:8]							
0x40010028 (GPIO0), 0x40011028 (GPIO1), 0x40013028 (GPIO2)	GPIO Controller	INTTYPESET	7:0	INTTYPESET[7:0]							
			15:8	INTTYPESET[15:8]							
0x4001002C (GPIO0), 0x4001102C (GPIO1), 0x4001302C (GPIO2)	GPIO Controller	INTTYPECLR	7:0	INTTYPECLR[7:0]							
			15:8	INTTYPECLR[15:8]							
0x40010030 (GPIO0), 0x40011030 (GPIO1), 0x40013030 (GPIO2)	GPIO Controller	INTPOLSET	7:0	INTPOLSET[7:0]							
			15:8	INTPOLSET[15:8]							
0x40010034 (GPIO0), 0x40011034 (GPIO1),	GPIO Controller	INTPOLCLR	7:0	INTPOLCLR[7:0]							
			15:8	INTPOLCLR[15:8]							

Absolute Address	Register Group	Name	Bit Pos.								
0x40013034 (GPIO2)											
0x40010038 (GPIO0), 0x40011038 (GPIO1), 0x40013038 (GPIO2)	GPIO Controller	INTSTATUSCLEAR	7:0	INTSTATUSCLEAR[7:0]							
			15:8	INTSTATUSCLEAR[15:8]							
0x4000B040	LPMCU_MISC_REGS0	INVERT_OUTPUT_CTRL	7:0	INVERT_OUT LP_GPIO_x (x = 7:0)							
			15:8	INVERT_OUT LP_GPIO_x (x = 15:8)							
			23:16	INVERT_OUT LP_GPIO_x (x = 23:16)							
			31:24	INVERT_OUT LP_SIP_x (x = 5:0)							INVERT_OUT LP_GPIO_24
0x4000B050	LPMCU_MISC_REGS0	PULL_ENABLE	7:0	PULL_EN LP_GPIO_x (x = 7:0)							
			15:8	PULL_EN LP_GPIO_x (x = 15:8)							
			23:16	PULL_EN LP_GPIO_x (x = 23:16)							
			31:24	PULL_EN LP_SIP_x (x = 5:0)							PULL_EN LP_GPIO_24
0x4000B054	LPMCU_MISC_REGS0	RTYPE_PAD_0	7:0	PULL_TYPE LP_GPIO_x (x = 7:0)							
			15:8	PULL_TYPE LP_GPIO_x (x = 15:8)							
			23:16	PULL_TYPE LP_GPIO_x (x = 23:16)							
			31:24								PULL_TYPE LP_GPIO_24
0x4000B414	LPMCU_MISC_REGS0	MS_GPIO	7:0	PULL_EN GPIO_MSy (y = 1:4)				PULL_TYPE GPIO_MSy (y = 1:4)			
0x4000F014	AON_GP_REGS0	AON_PULL_ENABLE	7:0						PULLUP_EN AO_GPIO_z (z= 0:2)		
0x4000E000	AON_PWR_SEQ0	GPIO_WAKEUP_CTRL	7:0							BLE_ENABLE	
0x4000B044	LPMCU_MISC_REGS0	PINMUX_SEL_0	7:0		PINMUX_SEL[2:0] LP_GPIO_1				PINMUX_SEL[2:0] LP_GPIO_0		
			15:8		PINMUX_SEL[2:0] LP_GPIO_3				PINMUX_SEL[2:0] LP_GPIO_2		
			23:16		PINMUX_SEL[2:0] LP_GPIO_5				PINMUX_SEL[2:0] LP_GPIO_4		
			31:24		PINMUX_SEL[2:0] LP_GPIO_7				PINMUX_SEL[2:0] LP_GPIO_6		
0x4000B048	LPMCU_MISC_REGS0	PINMUX_SEL_1	7:0		PINMUX_SEL[2:0] LP_GPIO_9				PINMUX_SEL[2:0] LP_GPIO_8		
			15:8		PINMUX_SEL[2:0] LP_GPIO_11				PINMUX_SEL[2:0] LP_GPIO_10		
			23:16		PINMUX_SEL[2:0] LP_GPIO_13				PINMUX_SEL[2:0] LP_GPIO_12		
			31:24		PINMUX_SEL[2:0] LP_GPIO_15				PINMUX_SEL[2:0] LP_GPIO_14		
0x4000B04C	LPMCU_MISC_REGS0	PINMUX_SEL_2	7:0		PINMUX_SEL[2:0] LP_GPIO_17				PINMUX_SEL[2:0] LP_GPIO_16		
			15:8		PINMUX_SEL[2:0] LP_GPIO_19				PINMUX_SEL[2:0] LP_GPIO_18		
			23:16		PINMUX_SEL[2:0] LP_GPIO_21				PINMUX_SEL[2:0] LP_GPIO_20		
			31:24		PINMUX_SEL[2:0] LP_GPIO_23				PINMUX_SEL[2:0] LP_GPIO_22		
0x4000B080	LPMCU_MISC_REGS0	PINMUX_SEL_4	7:0						PINMUX_SEL[2:0] LP_GPIO_24		
			15:8								
			23:16								
			31:24								
0x4000B1A0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_0	7:0			MEGAMUX_SEL[5:0] LP_GPIO_0					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_1					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_2					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_3					
0x4000B1A4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_1	7:0			MEGAMUX_SEL[5:0] LP_GPIO_4					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_5					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_6					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_7					

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B1A8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_2	7:0			MEGAMUX_SEL[5:0] LP_GPIO_8					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_9					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_10					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_11					
0x4000B1AC	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_3	7:0			MEGAMUX_SEL[5:0] LP_GPIO_12					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_13					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_14					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_15					
0x4000B1B0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_4	7:0			MEGAMUX_SEL[5:0] LP_GPIO_16					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_17					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_18					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_19					
0x4000B1B4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_5	7:0			MEGAMUX_SEL[5:0] LP_GPIO_20					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_21					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_22					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_23					
0x4000B1B8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_6	7:0			MEGAMUX_SEL[5:0] LP_GPIO_24					
0x4000F000	AON_GP_REGS0	AON_PINMUX_SEL	7:0			PINMUX_SEL[1:0] AO_GPIO_1				PINMUX_SEL[1:0] AO_GPIO_0	
			15:8							PINMUX_SEL[1:0] AO_GPIO_2	
0x4000F410	AON_GP_REGS0	MS_GPIO_MODE	7:0					ANALOG_EN GPIO_MS1	ANALOG_EN GPIO_MS2	ANALOG_EN GPIO_MS3	ANALOG_EN GPIO_MS4

12.11 Register Description

12.11.1 Data Input Value

Name: DATA
Reset: 0x---- (Based on level on I/O pin)

Absolute Address: 0x40010000 (GPIO0), 0x40011000 (GPIO1), 0x40013000 (GPIO2)

This register is a part of GPIO Controller registers. This register reads the input drive value on individual I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to register bit.

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 15:0 – DATA[15:0] Port Data Input Value

Read Value	Description
0	The corresponding I/O pin input sampler detects a logical low level on the input pin.
1	The corresponding I/O pin input sampler detects a logical high level on the input pin

Writing this register sends the DATA register value to DATAOUT register.

12.11.2 Data Output Value

Name: DATAOUT
Reset: 0x0000

Absolute Address: 0x40010004 (GPIO0), 0x40011004 (GPIO1), 0x40013004 (GPIO2)

This register is a part of GPIO Controller registers. This register sets the data output drive value for individual I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	DATAOUT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATAOUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATAOUT[15:0] Port Data Output Value
When the register is configured as output via the Data Direction register (OUTENSET), these bits set the logical output drive.

Read Value	Description
0	The corresponding I/O pin is driven logical low level.
1	The corresponding I/O pin is driven logical high level.

12.11.3 Data Direction Set

Name: OUTENSET
Reset: 0x0000

Absolute Address: 0x40010010 (GPIO0), 0x40011010 (GPIO1), 0x40013010 (GPIO2)

This register is a part of GPIO Controller registers. This register allows the user to set one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z) as an output. This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to register bit.

Bit	15	14	13	12	11	10	9	8
	OUTENSET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTENSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – OUTENSET[15:0] Port Data Direction Set
Writing '0' to a bit has no effect.

Writing '1' to a bit sets the corresponding bit in the OUTENSET register, which configures the I/O pin as an output.

Read Value	Description
0	Indicates the corresponding I/O pin in the GPIO Controller group as input.
1	Indicates the corresponding I/O pin in the GPIO Controller group as output.

12.11.4 Data Direction Clear

Name: OUTENCLR
Reset: 0x0000

Absolute Address: 0x40010014 (GPIO0), 0x40011014 (GPIO1), 0x40013014 (GPIO2)

This register is a part of GPIO Controller registers. This register allows the user to set one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z) as input. This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	OUTENCLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTENCLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – OUTENCLR[15:0] Port Data Direction Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit clears the corresponding bit in the OUTENSET register, which configures the I/O pin as an input.

Read Value	Description
0	Indicates the corresponding I/O pin in the GPIO Controller group as input.
1	Indicates the corresponding I/O pin in the GPIO Controller group as output.

12.11.5 Interrupt Enable Set

Name: INTENSET
Reset: 0x0000

Absolute Address: 0x40010020 (GPIO0), 0x40011020 (GPIO1), 0x40013020 (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to enable interrupt on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTENSET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTENSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTENSET[15:0] Interrupt Enable Set
Writing '0' to a bit has no effect.

Writing '1' to a bit sets the corresponding bit in the INTENSET register, which enables interrupt on I/O pin.

Read Value	Description
0	Indicates the interrupt is disabled on corresponding I/O pin in GPIO controller group.
1	Indicates the interrupt is enabled on corresponding I/O pin in GPIO controller group.

12.11.6 Interrupt Enable Clear

Name: INTENCLR
Reset: 0x0000

Absolute Address: 0x40010024 (GPIO0), 0x40011024 (GPIO1), 0x40013024 (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to disable interrupt on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTENCLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTENCLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTENCLR[15:0] Interrupt Enable Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit clears the corresponding bit in the INTENSET register, which disables interrupt on I/O pin.

Read Value	Description
0	Indicates the interrupt is disabled on corresponding I/O pin in GPIO controller group.
1	Indicates the interrupt is enabled on corresponding I/O pin in GPIO controller group.

12.11.7 Interrupt Type Set

Name: INTTYPESET
Reset: 0x0000

Absolute Address: 0x40010028 (GPIO0), 0x40011028 (GPIO1), 0x40013028 (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to set interrupt type on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTTYPESET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTTYPESET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTTYPESET[15:0] Interrupt Type Set
Writing '0' to a bit has no effect.

Writing '1' to a bit sets the corresponding bit in the INTTYPESET register, which configures interrupt as falling edge or rising edge. For more details, see Interrupt Configuration table.

Read Value	Description
0	Indicates the interrupt as LOW level or HIGH level decided by INTPOL register.
1	Indicates the interrupt as Falling edge or Rising edge decided by INTPOL register.

12.11.8 Interrupt Type Clear

Name: INTTYPECLR
Reset: 0x0000

Absolute Address: 0x4001002C (GPIO0), 0x4001102C (GPIO1), 0x4001302C (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to clear interrupt type on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTTYPECLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTTYPECLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTTYPECLR[15:0] Interrupt Type Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit clears the corresponding bit in the INTTYPESET register.

Read Value	Description
0	Indicates the interrupt as LOW level or HIGH level decided by INTPOL register.
1	Indicates the interrupt as Falling edge or Rising edge decided by INTPOL register.

12.11.9 Interrupt Polarity Set

Name: INTPOLSET
Reset: 0x0000

Absolute Address: 0x40010030 (GPIO0), 0x40011030 (GPIO1), 0x40013030 (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to set interrupt polarity on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTPOLSET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTPOLSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTPOLSET[15:0] Interrupt Polarity Set
Writing '0' to a bit has no effect.

Writing '1' to a bit sets the corresponding bit in the INTPOLSET register, which configures interrupt as High level or Rising edge. For more details, see Interrupt Configuration table.

Read Value	Description
0	Indicates the interrupt as LOW level or Falling edge decided by INTTYPE register.
1	Indicates the interrupt as HIGH level or Rising edge decided by INTTYPE register.

12.11.10 Interrupt Polarity Clear

Name: INTPOLCLR
Reset: 0x0000

Absolute Address: 0x40010034 (GPIO0), 0x40011034 (GPIO1), 0x40013034 (GPIO2)

This register is a part of GPIO Controller Registers. This register allows the user to clear interrupt polarity on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of the I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to the register bit.

Bit	15	14	13	12	11	10	9	8
	INTPOLCLR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTPOLCLR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTPOLCLR[15:0] Interrupt Polarity Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit clears the corresponding bit in the INTPOLSET register.

Read Value	Description
0	Indicates the interrupt as LOW level or Falling edge decided by INTTYPE register.
1	Indicates the interrupt as HIGH level or Rising edge decided by INTTYPE register.

12.11.11 Interrupt Status Clear

Name: INTSTATUSCLEAR
Reset: 0x0000

Absolute Address: 0x40010038 (GPIO0), 0x40011038 (GPIO1), 0x40013038 (GPIO2)

This register is a part of GPIO Controller Registers. This register indicates status of interrupt trigger and allows the user to clear interrupt status on one or more I/O pins (LP_GPIO_x, GPIO_MSy, AO_GPIO_z). This register is duplicated for each GPIO Controller, with increasing base address.

For more details on mapping between LP_GPIO_x, GPIO_MSy, AO_GPIO_z pin number with GPIO controller pin number, see GPIO Controller column of I/O Port Function Multiplexing table. The corresponding GPIO controller pin number 'n' is mapped to register bit.

Bit	15	14	13	12	11	10	9	8
	INTSTATUSCLEAR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTSTATUSCLEAR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTSTATUSCLEAR[15:0] Interrupt Status Clear
Writing '0' to a bit has no effect.

Writing '1' to a bit clears the interrupt request.

Read Value	Description
0	Indicates the interrupt request is not triggered.
1	Indicates the interrupt request is triggered.

12.11.12 LP_GPIO_x Invert Output Level

Name: INVERT_OUTPUT_CTRL
Reset: 0x00000000

Absolute Address: 0x4000B040

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to invert the logical output level which is set using DATAOUT register for LP_GPIO_x pins.

Bit	31	30	29	28	27	26	25	24
	INVERT_OUT LP_SIP_x	INVERT_OUT LP_SIP_x	INVERT_OUT LP_SIP_x	INVERT_OUT LP_SIP_x	INVERT_OUT LP_SIP_x			INVERT_OUT LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit	23	22	21	20	19	18	17	16
	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x	INVERT_OUT LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31,30,29,28,27 – INVERT_OUT LP_SIP_x (x = 4 to 0; Replace x=4 for bit 31, ... x=0 for bit 27) Output level invert
The LP_SIP_x pins are connected to internal SPI Flash0 which holds the application code. It is not recommended to use these pins as general purpose I/O.

Bits 24,23,22,21,20,19,18,17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – INVERT_OUT LP_GPIO_x (x = 24 to 0; Replace x=24 for bit 24, ... x=0 for bit 0) Output level invert
Writing '1'inverts the output logical level set using DATAOUT register on LP_GPIO_x pin. For example, if low level is set using DATAOUT register, writing '1' to INVERT_OUTPUT_CTRL changes to high level.

Writing '0' sets the output logical level same as DATAOUT register on LP_GPIO_x pin.

12.11.13 LP_GPIO_x Pull Enable

Name: PULL_ENABLE
Reset: 0x00000000

Absolute Address: 0x4000B050

This register is a part of LPMCU_MISC_REGS0 Registers. This register allows the user to enable or disable the internal pull up or pull down for LP_GPIO_x pins.

Bit	31	30	29	28	27	26	25	24
	PULL_EN LP_SIP_x	PULL_EN LP_SIP_x	PULL_EN LP_SIP_x	PULL_EN LP_SIP_x	PULL_EN LP_SIP_x			PULL_EN LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W			R/W
Reset	0	0	0	0	0			0

Bit	23	22	21	20	19	18	17	16
	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x	PULL_EN LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31,30,29,28,27 – PULL_EN LP_SIP_x (x = 4 to 0; Replace x=4 for bit 31, ... x=0 for bit 27) Pull Enable Register
The LP_SIP_x pins are connected to internal SPI Flash which holds the application code. It is not recommended to use these pins as general purpose I/O.

Bits 24,23,22,21,20,19,18,17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – PULL_EN LP_GPIO_x (x = 24 to 0; Replace x=24 for bit 24, ... x=0 for bit 0) Pull Enable Register
Writing '1'disables the internal Pull up/Pull down on LP_GPIO_x pin.

Writing '0' enables the internal Pull up/Pull down on LP_GPIO_x pin. It is an active LOW pull enable configuration.

12.11.14 LP_GPIO_x Pull Type Set

Name: RTYPE_PAD_0
Reset: 0x00000000

Absolute Address: 0x4000B054

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to set the pull type to pull up or pull down for LP_GPIO_x pins.

Bit	31	30	29	28	27	26	25	24
								PULL_TYPE LP_GPIO_x
Access								R/W
Reset								0

Bit	23	22	21	20	19	18	17	16
	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x	PULL_TYPE LP_GPIO_x
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 24,23,22,21,20,19,18,17,16,15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0 – PULL_TYPE LP_GPIO_x (x = 24 to 0; Replace x=24 for bit 24, ... x=0 for bit 0) Pull Type Set Register
Writing '1' enables the internal pull down on LP_GPIO_x pin.

Writing '0' enables the internal pull up on LP_GPIO_x pin.

12.11.15 GPIO_MSy Pull Configuration

Name: MS_GPIO
Reset: 0xF0

Absolute Address: 0x4000B414

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to set and enable the internal pull up or pull down for GPIO_MSy pins.

Bit	7	6	5	4	3	2	1	0
	PULL_EN GPIO_MSy	PULL_EN GPIO_MSy	PULL_EN GPIO_MSy	PULL_EN GPIO_MSy	PULL_TYPE GPIO_MSy	PULL_TYPE GPIO_MSy	PULL_TYPE GPIO_MSy	PULL_TYPE GPIO_MSy
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	0

Bits 7,6,5,4 – PULL_EN GPIO_MSy (y = 1 to 4; Replace y=1 for bit7, ... y=4 for bit4)
Writing '1'disables the internal pull up/pull down on GPIO_MSy pin.

Writing '0' enables the internal pull up/pull down on GPIO_MSy pin. It is an active LOW pull enable configuration.

Bits 3,2,1,0 – PULL_TYPE GPIO_MSy (y = 1 to 4; Replace y=1 for bit3, ... y=4 for bit0)
Writing '1' enables the internal pull down on GPIO_MSy pin.

Writing '0' disables the internal pull up on GPIO_MSy pin.

12.11.16 AO_GPIO_z Pull Enable

Name: AON_PULL_ENABLE
Reset: 0x00

Absolute Address: 0x4000F014

This register is a part of the AON_GP_REGS0 Registers. This register allows the user to enable the internal pull up for AO_GPIO_z pins.

Bit	7	6	5	4	3	2	1	0
						PULLUP_EN AO_GPIO_z	PULLUP_EN AO_GPIO_z	PULLUP_EN AO_GPIO_z
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2,1,0 – PULLUP_EN AO_GPIO_z (z = 2 to 0; Replace z=2 for bit 2, ... z=0 for bit0)
Writing '1'disables the internal pull up on AO_GPIO_z pin.

Writing '0' enables the internal pull up on AO_GPIO_z pin. It is an active LOW pull enable configuration

12.11.17 WakeUp Control on AO_GPIO_z

Name: GPIO_WAKEUP_CTRL
Reset: 0x02

Absolute Address: 0x4000E000

This register is a part of the AON_PWR_SEQ0 registers. This register allows the user to enable the AO_GPIO_z to wake-up BLE subsystem from the ULP mode.

Bit	7	6	5	4	3	2	1	0
							BLE_ENABLE	
Access							R/W	
Reset							1	

Bit 1 – BLE_ENABLE Wake-up BLE subsystem on AO_GPIO_z (z = 0,1,2)
Writing '0' to this bit disables the wake-up of BLE subsystem on AO_GPIO_z.

Writing '1' to this bit enables the wake-up of BLE subsystem on AO_GPIO_z. This configuration is common for all AO_GPIO_z pins.

For more details on wake-up procedure, see Wake-up Source.

13. Always-On (AON) Sleep Timer

This timer is a 32-bit countdown timer that operates on the 32 kHz sleep clock. It can be used as a general-purpose timer for the ARM or as a wake-up source for the chip.

13.1 Features

The following are the AON Sleep Timer features:

- 32 bit decrement counter operation
- Supported modes:
  - Single Count mode
  - Reload mode
- Wake-up source for ARM and BLE subsystem

13.2 Clock Configuration

The AON Sleep Timer must be provided with clock source before configuring for normal operation. For more details on configuration, see AON Sleep Timer Clock Configuration.

13.3 Functional Description

13.3.1 Initialization

After device reset, the AON Sleep Timer is not active.

13.3.2 Operation

The Always-On (AON) Sleep Timer generates a timer tick at a programmed interval. The counter decrements at the frequency of the P_CLK (32.768 kHz is configured) clock signal. For more details see, Clock Settings for Critical Sections. When the counter reaches zero, a tick is generated and interrupt is triggered.

There are two different modes; single count mode and reload mode. The following are the steps to initialize and enable the AON Sleep Timer.

- Counter is decremented for each P_CLK. Calculate the counter value for desired interval (ms) using the following formula:
  SINGLE_COUNT_DURATION = Interval (ms) * P_CLK (kHz)
- Load the counter value in SINGLE_COUNT_DURATION register.
- Configure the interrupt vector line to connect the interrupt request to NVIC. To use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. For more information, see Nested Vector Interrupt Controller.
- To enable timer with the Single Count mode, set SINGLE_COUNT_ENABLE bit in CONTROL register.
- To enable timer with the Reload mode, set RELOAD_ENABLE bit in CONTROL register. This loads the CURRENT_COUNT_VALUE register with the value set in SINGLE_COUNT_DURATION register. It is required to wait for reload delay (Reload mode) or single count delay (Single Count mode) to ensure that the timer is loaded with the set counter value.

- The CURRENT_COUNT_VALUE register starts decrementing and when it reaches zero, AON Sleep Timer interrupt is triggered. Interrupt request can be cleared by writing '1' to IRQ_CLEAR bit of CONTROL register.
- In Single Count mode, the AON Sleep Timer counter is not reloaded again and timer stops. In Reload mode AON Sleep Timer is again reloaded with SINGLE_COUNT_DURATION and timer starts decrementing again.

13.4 Restart the Running AON Sleep Timer

The AON Sleep Timer is started in Single Count mode or Reload mode by configuring CONTROL register as explained in Operation. Once the timer starts decrementing the CURRENT_COUNT_VALUE, to stop the counter, SINGLE_COUNT_ENABLE or RELOAD_ENABLE bit must be cleared. Even after clearing the bits, CURRENT_COUNT_VALUE register is not cleared immediately. It continues to decrement till it reaches zero, then the AON Sleep Timer stops.

Therefore, while restarting the timer again with new value loaded on SINGLE_COUNT_DURATION gets reloaded on CURRENT_COUNT_VALUE only when the current counter reaches zero.

AON Sleep Timer must be reset to clear the CURRENT_COUNT_VALUE to zero immediately. The AON Sleep Timer can be reset by clearing the SLEEP_TIMER_RSTN bit of AON_GLOBAL_RESET register. This procedure resets all the AON Sleep Timer registers to default values. For more details, see AON Sleep Timer Reset.

The AON Sleep Timer must be disabled before it is reset in order to avoid undefined behavior.

13.5 Wake-up Source

The AON Sleep Timer is also a wake-up source for the ARM subsystem and BLE subsystem to wake-up from the ULP mode after the set interval. Enabling the AON Sleep Timer as wake-up source can be done using the AON_ST_WAKEUP_CTRL register. By default, on reset the AON Sleep Timer as wake-up source is disabled.

Note: It is recommended to enable wake-up of ARM subsystem and BLE subsystem together or wake-up of only the ARM subsystem. Enabling only the wake-up of the BLE subsystem should not be performed.

13.6 Power Management

As AON Timer belongs to the Always On power domain, the configuration registers are intact when device goes to the ULP mode. For more details on how sleep and wake-up are controlled by ROM firmware, see ATSAMB11 BluSDK Smart Interrupts and ULP Architecture.

13.7 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x4000D000	AON_SLEEP_TIMER0	CONTROL	7:0				IRQ_CLEAR			SINGLE_COUNT_ENABLE	RELOAD_ENABLE
			15:8		SLP_TIMER_SINGLE_COUNT_ENABLE_DLY [2:0]					SLP_TIMER_CLK_RELOAD_DLY[1:0]	

Absolute Address	Register Group	Name	Bit Pos.								
			23:16								
			31:24	SLEEP_TIMER_NOT_ACTIVE	SLEEP_TIMER_ACTIVE						
0x4000D004	AON_SLEEP_TIMER0	SINGLE_COUNT_DURATION	7:0	COUNT_DURATION[7:0]							
			15:8	COUNT_DURATION[15:8]							
			23:16	COUNT_DURATION[23:16]							
			31:24	COUNT_DURATION[31:24]							
0x4000D00C	AON_SLEEP_TIMER0	CURRENT_COUNT_VALUE	7:0	COUNT[7:0]							
			15:8	COUNT[15:8]							
			23:16	COUNT[23:16]							
			31:24	COUNT[31:24]							
0x4000E00C	AON_PWR_SEQ0	AON_ST_WAKEUP_CTRL	7:0							BLE_ENABLE	ARM_ENABLE

13.8 Register Description

13.8.1 AON Sleep Timer Control

Name: CONTROL
Reset: 0x80000000

Absolute Address: 0x4000D000

This register is a part of AON_SLEEP_TIMER0 Registers. This register allows the user to configure and enable AON Sleep Timer in Single Count mode or Reload mode.

Bit	31	30	29	28	27	26	25	24
	SLEEP_TIMER_NOT_ACTIVE	SLEEP_TIMER_ACTIVE						
Access	R	R						
Reset	1	0						

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2:0]					SLP_TIMER_CLK_RELOAD_DLY[1:0]	
Access		R	R	R			R	R
Reset		0	0	0			0	0

Bit	7	6	5	4	3	2	1	0
				IRQ_CLEAR			SINGLE_COUNT_ENABLE	RELOAD_ENABLE
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 31 – SLEEP_TIMER_NOT_ACTIVE
Read value '1', indicates that the CURRENT_COUNT_VALUE is 0 and AON Sleep Timer is not active.

Bit 30 – SLEEP_TIMER_ACTIVE
Read value '1', indicates that the CURRENT_COUNT_VALUE value is not 0 and AON Sleep Timer is running.

Bits 14:12 – SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2:0]
This provides the current status of the Single Count mode. Before setting or clearing SINGLE_COUNT_ENABLE bit the SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2] bit must be checked.

Read Value of SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2]	Description
0	If SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2] is 0, which means the SINGLE_COUNT_ENABLE bit is cleared and can write SINGLE_COUNT_ENABLE bit to a 1 when needed
1	If SLP_TIMER_SINGLE_COUNT_ENABLE_DLY[2] is 1, which means the SINGLE_COUNT_ENABLE bit is set and can write SINGLE_COUNT_ENABLE bit to a 0 when needed

Bits 9:8 – SLP_TIMER_CLK_RELOAD_DLY[1:0]
This provides the current status of the reload mode. Before setting or clearing RELOAD_ENABLE bit the SLP_TIMER_CLK_RELOAD_DLY[1] bit must be checked.

Read Value of SLP_TIMER_CLK_RELOAD_DLY[1]	Description
0	If SLP_TIMER_CLK_RELOAD_DLY[1] bit is 0, which means the RELOAD_ENABLE bit is cleared and it is safe to write RELOAD_ENABLE bit to a 1 when needed
1	If SLP_TIMER_CLK_RELOAD_DLY[1] bit is 1, which means the RELOAD_ENABLE bit is set and it is safe to write RELOAD_ENABLE bit to a 0 when needed

Bit 4 – IRQ_CLEAR
Writing '0' to a bit has no effect.

Writing '1' to a bit will clear the AON Sleep Timer interrupt request.

Bit 1 – SINGLE_COUNT_ENABLE
Writing '0' to a bit disables AON Sleep Timer in Single Count mode.

Writing '1' to a bit enables AON Sleep Timer in Single Count mode and loads the AON Sleep Timer with the SINGLE_COUNT_DURATION value.

Bit 0 – RELOAD_ENABLE
Writing '0' to a bit disables AON Sleep Timer in Reload mode.

Writing '1' to a bit enable AON Sleep Timer in Reload mode and loads the AON Sleep Timer with the SINGLE_COUNT_DURATION value whenever the timer expires.

13.8.2 AON Sleep Timer Duration

Name: SINGLE_COUNT_DURATION
Reset: 0x00000000

Absolute Address: 0x4000D004

This register is a part of AON_SLEEP_TIMER0 Registers. This register allows the user to load AON Sleep Timer duration counter value for Single Count mode or Reload mode.

Bit	31	30	29	28	27	26	25	24
	COUNT_DURATION[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT_DURATION[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT_DURATION[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT_DURATION[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT_DURATION[31:0]
These bits hold the counter value equivalent to timer interval that is loaded into the CURRENT_COUNT_VALUE register. For more details on formula, see Operation.

13.8.3 AON Sleep Timer Current Counter Value

Name: CURRENT_COUNT_VALUE
Reset: 0x00000000

Absolute Address: 0x4000D00C

This register is a part of the AON_SLEEP_TIMER0 Registers. This register contains the AON Sleep Timer current counter value of Single Count mode or Reload mode. This starts decrementing and when it reaches zero AON Sleep Timer interrupt is triggered.

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0]
These bits contain the current counter value.

13.8.4 WakeUp Control on AON Sleep Timer

Name: AON_ST_WAKEUP_CTRL
Reset: 0x00

Absolute Address: 0x4000E00C

This register is a part of the AON_PWR_SEQ0 Registers. This register allows the user to enable the AON Sleep Timer to wake-up ARM subsystem and BLE subsystem from the ULP mode.

Bit	7	6	5	4	3	2	1	0
							BLE_ENABLE	ARM_ENABLE
Access							R/W	R/W
Reset							0	0

Bit 1 – BLE_ENABLE
Writing '0' disables BLE subsystem wake-up by AON Sleep Timer.

Writing '1' enables BLE subsystem wake-up by AON Sleep Timer.

Bit 0 – ARM_ENABLE
Writing '0' disables ARM subsystem wake-up by AON Sleep Timer.

Writing '1' enables ARM subsystem wake-up by AON Sleep Timer.

14. Pulse Width Modulation

The Pulse Width Modulation (PWM) feature provides a way to generate a periodic pulse waveform. The SAMB11 contains four individually configurable PWM blocks to provide external control voltages.

14.1 Features

- Four individually configurable PWM blocks
- Automatic generation of PWM output by hardware without software intervention
- Two PWM modes of operation
- Configurable period and duty cycle of PWM output
- Four different selectable base frequencies for PWM (26 MHz, 13 MHz, 6.5 MHz, 3.25 MHz)
- Configurable PWM output on LP_GPIO_x pins via MEGAMUX options

14.2 Clock Configuration

Before configuring the PWM registers, reset the PWM core by setting PWMx_ RSTN bit in LPMCU_GLOBAL_RESET_0 register. The PWM peripheral must be provided with clock source before configuring for normal operation. For more details on configuration, see Peripheral Clock Configuration.

14.3 Functional Description

14.3.1 Initialization

After device reset, PWM registers are zero.

PWM waveform can be output on any of LP_GPIO_x pins configured through MEGAMUX options.

- To get output of PWM waveform on specific LP_GPIO_x pin, configure PINMUX_SEL[2:0] of specific pin on PINMUX_SEL_n register with value equal to 1. This configuration enables MEGAMUXing on this pin.
- See the MEGAMUX Options table and configure the MEGA_MUX_IO_SEL_n register with PWM option.
- Select the PWM module clock source by configuring the CLOCK_SEL[1:0] bits of PWMn_CTRL register. The clock sources that can be selected are 26 MHz, 13 MHz, 6.5 MHz and 3 MHz.
- There are two modes of operation that are selectable through the PWM_MODE_SEL bit of the PWMn_CTRL register.
  - PWM Mode 1–Clear PWM_MODE_SEL bit
  - PWM Mode 2–Set PWM_MODE_SEL bit

14.3.2 PWM Mode 1 Operation

The PWM Mode 1 operation is based on 15-bit timer with compare match logic. The PWM period (T) is controlled by PWM_PERIOD [3:0] and the duty cycle is controlled by AGCDATA_IN[9:0] bits of PWMn_CTRL register. The timer TOP value is set based on PWM_PERIOD[3:0] and SAMPLE_METHOD as shown in the following table. When the PWM is enabled by writing 1’ to PWM_EN bit of PWMn_CTRL register, the timer counter is incremented for every clock cycle. When up-counting, the PWM output on LP_GPIO_x is set when the masked value of TOP value with timer counter becomes ZERO. The PWM

output is cleared when the timer counter reaches CC value as per the table. This PWM output polarity on LP_GPIO_x is reversed when OUTPUT_POLARITY bit of PWMn_CTRL register is set.

14.3.2.1 Method of Operation in PWM Mode 1

There are three methods of operation in PWM Mode 1:

1. USE_AGCUPDATE=1 and AGCUPDATE=1
2. USE_AGCUPDATE=0 , AGCUPDATE=0 and SAMPLE_METHOD=1
3. USE_AGCUPDATE=0 , AGCUPDATE=0 and SAMPLE_METHOD=0

Table 14-1. PWM Mode 1 Functional Values

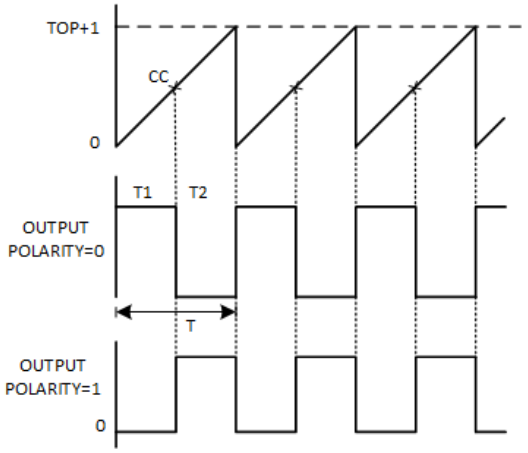
PWM_PERIOD[3:0]	CC	SHIFTED_OUT			TOP			MAX		
		SAMPLE_METHOD=0	SAMPLE_METHOD=1	USE_AGCUPDATE = 1, AGC_UPDATE=1	SAMPLE_METHOD=0	SAMPLE_METHOD=1	USE_AGCUPDATE = 1, AGC_UPDATE=1	SAMPLE_METHOD=0	SAMPLE_METHOD=1	USE_AGCUPDATE = 1, AGC_UPDATE=1
0	AGCDATA_IN_POST_INVERT[9:0]>>4	AGCDATA_IN_POST_INVERT[3:0]	0	0	0x3F	0x3F	0x3F	0x3FF	0x3F	0x3F
1	AGCDATA_IN_POST_INVERT[9:0]>>3	AGCDATA_IN_POST_INVERT[2:0]	0	0	0x7F	0x7F	0x7F	0x3FF	0x7F	0x7F
2	AGCDATA_IN_POST_INVERT[9:0]>>2	AGCDATA_IN_POST_INVERT[1:0]	0	0	0xFF	0xFF	0xFF	0x3FF	0xFF	0xFF
3	AGCDATA_IN_POST_INVERT[9:0]>>1	AGCDATA_IN_POST_INVERT[0:0]	0	0	0x1FF	0x1FF	0x1FF	0x3FF	0x1FF	0x1FF
4	AGCDATA_IN_POST_INVERT[9:0]>>0	0	0	0	0x3FF	0x3FF	0x3FF	0x3FF	0x3FF	0x3FF
5	AGCDATA_IN_POST_INVERT[9:0]<<1	0	0	0	0x7FF	0x7FF	0x7FF	0x3FF	0x7FF	0x7FF
6	AGCDATA_IN_POST_INVERT[9:0]<<2	0	0	0	0xFFF	0xFFF	0xFFF	0x3FF	0xFFF	0xFFF
7	AGCDATA_IN_POST_INVERT[9:0]<<3	0	0	0	0x1FFF	0x1FFF	0x1FFF	0x3FF	0x1FFF	0x1FFF
8	AGCDATA_IN_POST_INVERT[9:0]<<4	0	0	0	0x3FFF	0x3FFF	0x3FFF	0x3FF	0x3FFF	0x3FFF
Others	AGCDATA_IN_POST_INVERT[9:0]>>0	0	0	0	0x3FF	0x3FF	0x3FF	0x3FF	0x3FF	0x3FF

Note: The AGCDATA_FMT bit of PWMn_CTRL register decides the sign of AGCDATA_IN[9:0] data. If AGCDATA_FMT is '1' then AGCDATA_IN is unsigned data and if AGCDATA_FMT is '0' then AGCDATA_IN is signed data.
AGCDATA_IN_POST_INVERT[9:0] = {AGCDATA_IN[9] ^ (~AGCDATA_FMT), AGCDATA_IN[8:0]}

USE_AGCUPDATE=1 and AGCUPDATE=1

If USE_AGCUPDATE bit is '1', then the AGCUPDATE bit must be '1' for PWM pulse output. The TOP and MAX values are as per PWM Mode 1 Functional Values under USE_AGCUPDATE =1, AGCUPDATE=1. The TOP and MAX values are same in this method. The CC value is the shifted value of AGCDATA_IN[9:0]. The SHIFTED_OUT bits of AGCDATA_IN[9:0] are lost in this method. Hence, there PWM pulse output is not generated for AGCDATA_IN[9:0] values 0x1 to 0xF.

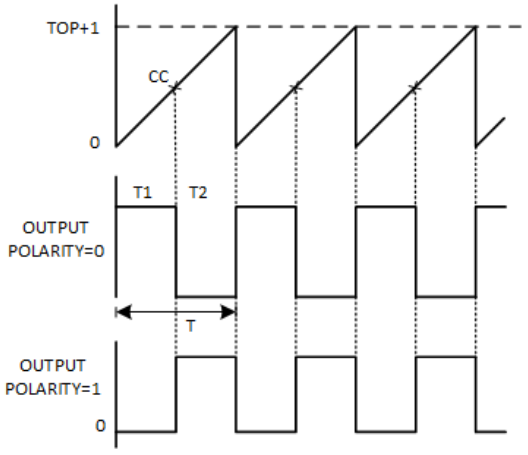
Figure 14-1. PWM Mode1 Operation USE_AGCUPDATE=0 , AGCUPDATE=0 and SAMPLE_METHOD=1



USE_AGCUPDATE=0 , AGCUPDATE=0 and SAMPLE_METHOD=1

If USE_AGCUPDATE is '0', then PWM pulse output is changed based on SAMPLE_METHOD bit. Refer the TOP and MAX in table under SAMPLE_METHOD=1. The operation of SAMPLE_METHOD=1 is same as the first method.

Figure 14-2. PWM Mode1 Operation USE_AGCUPDATE =1 and AGCUPATE=1



USE_AGCUPDATE=0 , AGCUPDATE=0 and SAMPLE_METHOD=0

If USE_AGCUPDATE is '0' and SAMPLE_METHOD=0, then, the TOP and MAX values are referred under SAMPLE_METHOD=0 in table. The TOP and MAX values are not same in this method. In this method, the SHIFTED_OUT bits of AGCDATA_IN adds extra cycle in the PWM pulse stream. The SHIFTED_OUT value is getting added with EXTRA_CYCLE[3:0] every time the counter reaches TOP

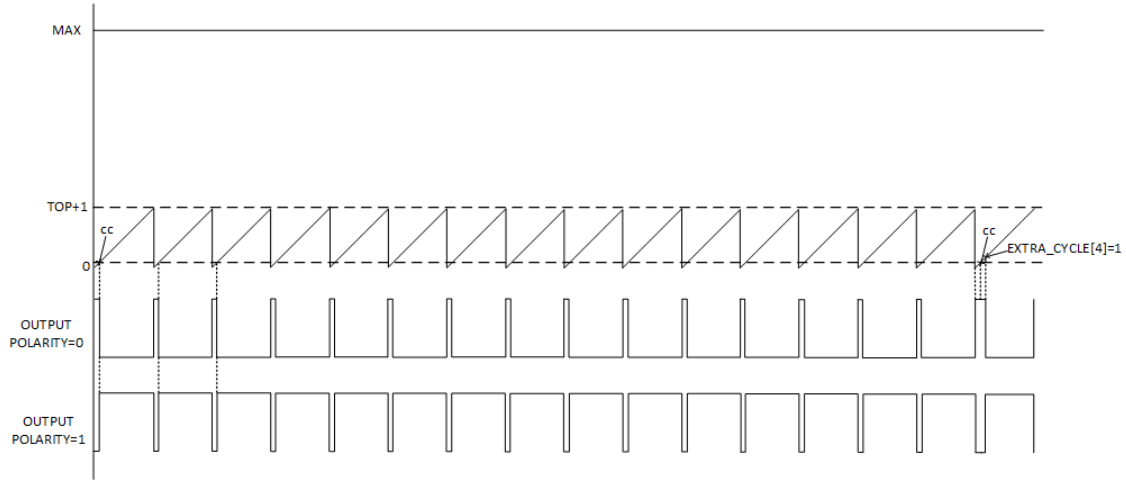
value as per the following equation. An extra pulse is generated when the bit ‘4’ of EXTRA_CYCLE[4:0] is set.

EXTRA_CYCLE[4:0] = SHITED_OUT + EXTRA_CYCLE[3:0]

Example1: The PWM pulse output for AGCDATA_IN[9:0] = 0x11 and PWM_PERIOD[3:0]=0x00 is shown in the following figure. When upcounting, the PWM output on LP_GPIO_x is set when the masked value of TOP (TOP = 0x3F) value with timer counter becomes ZERO. The PWM output is cleared when the timer counter reaches CC (CC = 0x01). An extra cycle is added in the pulse stream when EXTRA_CYCLE[4:0] bit '4' is set. This is set when timer counter reaches 0x3CO for this AGCDATA_IN[9:0] = 0x11 as shown in the following figure.

Figure 14-3. PWM Mode1 Operation SAMPLE_METHOD=0

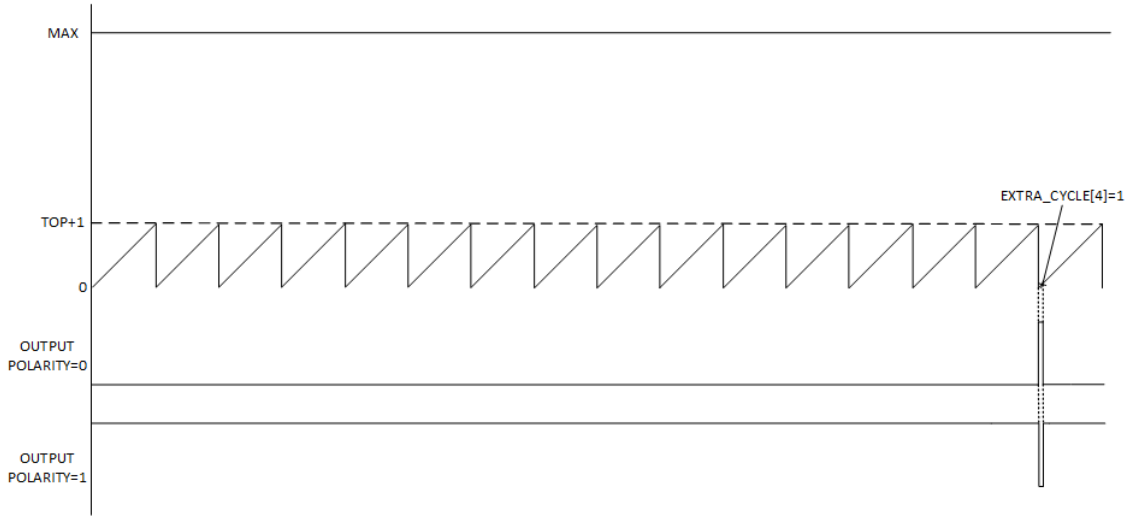
Example: AGCDATA_IN[9:0] = 0x11 and PWM_PERIOD[3:0] = 0



Example2: The PWM pulse output for AGCDATA_IN[9:0] = 0x01 and PWM_PERIOD[3:0]=0x00 is shown in the following figure. As CC=0x00, there is no pulse stream, but an extra cycle is added in the pulse stream when EXTRA_CYCLE[4:0] bit '4' is set. The extra pulse is added when timer counter reaches 0x3CO for this AGCDATA_IN[9:0] = 0x01 as shown in the following figure.

Figure 14-4. Figure 14-3. PWM Mode1 Operation SAMPLE_METHOD=0

Example: AGCDATA_IN[9:0] = 0x01 and PWM_PERIOD[3:0] = 0



14.3.2.2 PWM Pulse Frequency

The clock input to PWM module can be selected through CLOCK_SEL[1:0] bits of PWMn_CTRL register. Four different clock inputs are possible. The PWM pulse frequency (f_{PWM}) of the PWM block is derived from selected input clock frequency (f_{PWM_base}) using the following formula.

When, PWM_PERIOD[3:0] = 0,1,2, … , 8

$$f_{PWM}(\text{Mode 1}) = \frac{f_{PWM\_base}}{64*2^{\text{PWM\_PERIOD[3:0]}}}$$

When, PWM_PERIOD[3:0] > 8

$$f_{PWM}(\text{Mode 1}) = \frac{f_{PWM\_base}}{64*2\text{^}4}$$

f_{PWM_base} can be selected to have different values according to Table 14-2. The minimum and maximum frequencies supported for each clock selection are also listed in the table.

Table 14-2. f_{PWM} Range for Different f_{PWM} Base Frequencies

f_{PWM_base}	f_{PWM} max.	f_{PWM} min.
26 MHz	406.25 kHz	1.586 kHz
13 MHz	203.125 kHz	793.25 Hz
6.5 MHz	101.562 kHz	396.72 Hz
3.25 MHz	50.781 kHz	198.36 Hz

14.3.2.3 PWM Duty Cycle

The duty cycle is configured through AGCDATA_IN[9:0] bits. The duty cycle is calculated using the following formula:

$$\text{Duty cycle (Mode1)} = \frac{\text{CC}}{\text{TOP}+1}$$

14.3.2.4 Enabling and Disabling PWM Mode 1 Operation

After configuring PWMn_CTRL register with desired duty cycle and period the PWM output on specific LP_GPIO_x is enabled by writing a ‘1’ to PWM_EN bit of PWMn_CTRL register.

14.3.2.5 Updating New Duty Cycle and Period for Mode 1

USE_AGCUPDATE and AGCUPDATE decide the update new AGCDATA_IN[9:0] value and output the PWM pulse accordingly. If USE_AGCUPDATE is ‘1’ then only when AGCUPDATE bit is ‘1’ the AGCDATA_IN[9:0] is loaded into internal registers. The PWM output is available on LP_GPIO_x pin after PWM_EN is set. If AGCUPDATE bit is ‘0’ then PWM pulse is not output.

If USE_AGCUPDATE is ‘0’ then the internal PWM register is updated with new values when the timer counter reaches MAX value in SAMPLE_METHOD =1 and SAMPLE_METHOD =0.

14.3.3 PWM Mode 2 Operation

The PWM Mode 2 operation is based on accumulator logic. Both the PWM period (T) and duty cycle are controlled by AGCDATA_IN[9:0] bits of PWMn_CTRL register. The PWM Mode 2 operation is selected by setting PWM_MODE_SEL bit of PWMn_CTRL register. When AGCUPDATE bit is ‘1’ the AGCDATA_IN_POST_INVERT[9:0] is loaded into internal register. Enable PWM pulse output on specific LP_GPIO_x by writing a ‘1’ to PWM_EN bit of PWMn_CTRL register. When AGCUPDATE bit is ‘0’, on

every clock cycle (clock input selected using CLOCK_SEL[2:0] bits of PWMn_CTRL register) accumulation happens as per below calculation:

AGC_ACC[10:0] = AGCDATA_IN_POST_INVERT[9:0] + AGC_ACC[9:0]

The PWM output on LP_GPIO_x is set whenever AGC_ACC[10] is '1' and cleared when AGC_ACC[10] is '0'. This PWM output polarity on LP_GPIO_x is reversed when OUTPUT_POLARITY bit of PWMn_CTRL register is set.

14.3.3.1 PWM Pulse Frequency

The clock input to PWM module can be selected through CLOCK_SEL[1:0] bits of PWMn_CTRL register. Four different clock inputs are possible. The PWM pulse frequency (f_{PWM}) of the PWM block is derived from selected input clock frequency (f_{PWM_base}) using following formula.

When, AGCDATA_IN_POST_INVERT[9:0] <= 512:

$$f_{PWM}(\text{Mode 2}) = f_{PWM\_base} * \text{AGCDATA\_IN\_POST\_INVERT}[9:0]/1024$$

When, AGCDATA_IN_POST_INVERT[9:0] > 512:

$$f_{PWM}(\text{Mode 2}) = f_{PWM\_base} * (1024 - \text{AGCDATA\_IN\_POST\_INVERT}[9:0])/1024$$

Note: The AGCDATA_FMT bit of PWMn_CTRL register decides the sign of AGCDATA_IN[9:0] data. If AGCDATA_FMT is '1' then AGCDATA_IN is unsigned data and if AGCDATA_FMT is '0' then AGCDATA_IN is signed data.
AGCDATA_IN_POST_INVERT[9:0] = {AGCDATA_IN[9] ^ (~AGCDATA_FMT), AGCDATA_IN[8:0]}

14.3.3.2 PWM Duty Cycle

The duty cycle is configured through AGCDATA_IN[9:0] bits. The duty cycle is calculated using the following formula:

$$\text{Duty cycle (Mode2)} = \frac{\text{AGCDATA\_IN\_POST\_INVERT}[9:0]}{1024}$$

Note: The AGCDATA_FMT bit of PWMn_CTRL register decides the sign of AGCDATA_IN[9:0] data. If AGCDATA_FMT is '1' then AGCDATA_IN is unsigned data and if AGCDATA_FMT is '0' then AGCDATA_IN is signed data.
AGCDATA_IN_POST_INVERT[9:0] = {AGCDATA_IN[9] ^ (~AGCDATA_FMT), AGCDATA_IN[8:0]}

14.3.3.3 Enabling and Disabling PWM Mode 2 Operation

After configuring PWMn_CTRL register with desired duty cycle and period the PWM output on specific LP_GPIO_x is enabled by writing a '1' to PWM_EN bit of PWMn_CTRL register.

14.3.3.4 Updating New Duty Cycle and Period

The AGCUPDATE bit decides the update of new AGCDATA_IN[9:0] and output of the PWM pulse accordingly. If AGCUPDATE bit is '1', the AGCDATA_IN[9:0] will be loaded into internal register. If AGCUPDATE bit is '0', the AGC accumulation as per new AGCDATA_IN[9:0] value starts and PWM pulse is available on LP_GPIO_x pin when PWM_EN is bit is set. The USE_AGCUPDATE bit is not used for PWM Mode 2 operation.

14.4 Power Management

If the system goes to the Ultra-Low Power mode, the PWM peripheral is shut down and the PWM pulse output is stopped. The PWM configuration registers lose its content, and can not be restored when powered-up again. Therefore, the user must reconfigure the PWM peripheral at power-up to ensure it is in a well-defined state before use. For details on reconfiguration, refer to ATSAMB11 BluSDK Smart

Interrupts and ULP Architecture and Usage User Guide. This document also explains how sleep and wake-up are controlled.

14.5 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B160	LPMCU_MISC_REGS0 Registers	PWM0_CTRL	7:0	PWM_PERIOD[2:0]	PWM_MODE_SEL			SAMPLE_METHOD	AGCDATA_FMT	OUTPUT_POLARITY	PWM_EN
			15:8	AGCDATA_IN[6:0]							PWM_PERIOD[3]
			23:16		CLOCK_SEL[1:0]		AGC_UPDATE	USE_AGCUPDATE	AGCDATA_IN[9:7]		
0x4000B164	LPMCU_MISC_REGS0 Registers	PWM1_CTRL	7:0	PWM_PERIOD[2:0]	PWM_MODE_SEL			SAMPLE_METHOD	AGCDATA_FMT	OUTPUT_POLARITY	PWM_EN
			15:8	AGCDATA_IN[6:0]	PWM_PERIOD[3]						
			23:16		CLOCK_SEL[1:0]		AGC_UPDATE	USE_AGCUPDATE	AGCDATA_IN[9:7]		
0x4000B168	LPMCU_MISC_REGS0 Registers	PWM2_CTRL	7:0	PWM_PERIOD[2:0]	PWM_MODE_SEL			SAMPLE_METHOD	AGCDATA_FMT	OUTPUT_POLARITY	PWM_EN
			15:8	AGCDATA_IN[6:0]	PWM_PERIOD[3]						
			23:16		CLOCK_SEL[1:0]		AGC_UPDATE	USE_AGCUPDATE	AGCDATA_IN[9:7]		
0x4000B16C	LPMCU_MISC_REGS0 Registers	PWM3_CTRL	7:0	PWM_PERIOD[2:0]	PWM_MODE_SEL			SAMPLE_METHOD	AGCDATA_FMT	OUTPUT_POLARITY	PWM_EN
			15:8	AGCDATA_IN[6:0]	PWM_PERIOD[3]						
			23:16		CLOCK_SEL[1:0]		AGC_UPDATE	USE_AGCUPDATE	AGCDATA_IN[9:7]		
0x4000B044	LPMCU_MISC_REGS0	PINMUX_SEL_0	7:0		PINMUX_SEL[2:0] LP_GPIO_1				PINMUX_SEL[2:0] LP_GPIO_0		
			15:8		PINMUX_SEL[2:0] LP_GPIO_3				PINMUX_SEL[2:0] LP_GPIO_2		
			23:16		PINMUX_SEL[2:0] LP_GPIO_5				PINMUX_SEL[2:0] LP_GPIO_4		
			31:24		PINMUX_SEL[2:0] LP_GPIO_7				PINMUX_SEL[2:0] LP_GPIO_6		
0x4000B048	LPMCU_MISC_REGS0	PINMUX_SEL_1	7:0		PINMUX_SEL[2:0] LP_GPIO_9				PINMUX_SEL[2:0] LP_GPIO_8		
			15:8		PINMUX_SEL[2:0] LP_GPIO_11				PINMUX_SEL[2:0] LP_GPIO_10		
			23:16		PINMUX_SEL[2:0] LP_GPIO_13				PINMUX_SEL[2:0] LP_GPIO_12		
			31:24		PINMUX_SEL[2:0] LP_GPIO_15				PINMUX_SEL[2:0] LP_GPIO_14		
0x4000B04C	LPMCU_MISC_REGS0	PINMUX_SEL_2	7:0		PINMUX_SEL[2:0] LP_GPIO_17				PINMUX_SEL[2:0] LP_GPIO_16		
			15:8		PINMUX_SEL[2:0] LP_GPIO_19				PINMUX_SEL[2:0] LP_GPIO_18		
			23:16		PINMUX_SEL[2:0] LP_GPIO_21				PINMUX_SEL[2:0] LP_GPIO_20		
			31:24		PINMUX_SEL[2:0] LP_GPIO_23				PINMUX_SEL[2:0] LP_GPIO_22		
0x4000B080	LPMCU_MISC_REGS0	PINMUX_SEL_4	7:0						PINMUX_SEL[2:0] LP_GPIO_24		
			15:8								
			23:16								
			31:24								
0x4000B1A0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_0	7:0		MEGAMUX_SEL[5:0] LP_GPIO_0						
			15:8		MEGAMUX_SEL[5:0] LP_GPIO_1						
			23:16		MEGAMUX_SEL[5:0] LP_GPIO_2						
			31:24		MEGAMUX_SEL[5:0] LP_GPIO_3						
0x4000B1A4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_1	7:0		MEGAMUX_SEL[5:0] LP_GPIO_4						
			15:8		MEGAMUX_SEL[5:0] LP_GPIO_5						
			23:16		MEGAMUX_SEL[5:0] LP_GPIO_6						

Absolute Address	Register Group	Name	Bit Pos.								
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_7					
0x4000B1A8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_2	7:0			MEGAMUX_SEL[5:0] LP_GPIO_8					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_9					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_10					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_11					
0x4000B1AC	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_3	7:0			MEGAMUX_SEL[5:0] LP_GPIO_12					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_13					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_14					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_15					
0x4000B1B0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_4	7:0			MEGAMUX_SEL[5:0] LP_GPIO_16					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_17					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_18					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_19					
0x4000B1B4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_5	7:0			MEGAMUX_SEL[5:0] LP_GPIO_20					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_21					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_22					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_23					
0x4000B1B8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_6	7:0			MEGAMUX_SEL[5:0] LP_GPIO_24					

14.6 Register Description

14.6.1 PWM Control Register

Name: PWMn_CTRL
Reset: 0x000000

Absolute Address: 0x4000B160(PWM0),0x4000B164(PWM1),0x4000B168(PWM2), 0x4000B16C(PWM3)

This register is a part of the LPMCU_MISC_REGS0 Registers. This register allows the user to configure PWM functionality and enables the PWM output. There are four individual PWM blocks in SAMB11 and four PWMn_CTRL registers (n=0,1,2,3).

Bit	23	22	21	20	19	18	17	16
		CLOCK_SEL[1:0]		AGC_UPDATE	USE_AGCUPDATE	AGCDATA_IN[9:7]		
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	AGCDATA_IN[6:0]							PWM_PERIOD[3:3]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PWM_PERIOD[2:0]			PWM_MODE_SEL	SAMPLE_METHOD	AGCDATA_FMT	OUTPUT_POLARITY	PWM_EN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:21 – CLOCK_SEL[1:0]
These bits select clock input for PWM.

CLOCK_SEL[1:0]	Description
0x0	26 MHz
0x1	13 MHz
0x2	6.5 MHz
0x3	3.25 MHz

Bit 20 – AGC_UPDATE
In combination with USE_AGCUPDATE, PWM_MODE_SEL, and SAMPLE_METHOD controls the loading of AGCDATA_IN into internal registers.

Bit 19 – USE_AGCUPDATE
In combination with AGC_UPDATE, and PWM_MODE_SEL controls the loading of AGCDATA_IN into internal registers.

PWM_MODE_SEL	USE_AGCUPDATE	AGC_UPDATE	SAMPLE_METHOD	Operation
0	1	1	X	AGCDATA_IN loaded into internal register
0	1	0	X	AGCDATA_IN is not loaded into internal register
0	0	X	1	The SHIFTED_OUT bits of AGCDATA_IN[9:0] are lost in this method
0	0	X	0	The SHIFTED_OUT bits of AGCDATA_IN adds extra cycle in the PWM pulse stream
1	X	0->1->0	X	AGCDATA_IN loaded into internal register when AGC_UPDATE is '1' and PWM output is seen after AGC_UPDATE is made as '0'

Bits 18:9 – AGCDATA_IN[9:0]
Configures the duty cycle.

Bits 8:5 – PWM_PERIOD[3:0]
Configures the period of PWM pulse frequency for PWM Mode 1 operation. For more details on formula, see PWM Pulse Frequency.

Bit 4 – PWM_MODE_SEL
Selects the two different PWM modes of operations.

PWM_MODE_SEL	Mode
0	Mode 1
1	Mode 2

Bit 3 – SAMPLE_METHOD

SAMPLE_METHOD	Description
0	SHIFTED_OUT bits of AGCDATA_IN adds extra cycle in the PWM pulse stream
1	The SHIFTED_OUT bits of AGCDATA_IN[9:0] are lost in this method

Bit 2 – AGCDATA_FMT
Configures the sign of AGCDATA_IN[9:0] value.

Bit 1 – OUTPUT_POLARITY
Writing '1' to this bit reverses PWM pulse output polarity.

Bit 0 – PWM_EN
Writing '1' to this bit enables PWM functionality.

Writing '0' to this bit disables PWM functionality.

15. I²C Interface

The ATSAMB11-XR2100A and the ATSAMB11-ZR210CA provide an I²C interface that can be configured as slave or master. The I²C interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The ATSAMB11-XR2100A and the ATSAMB11-ZR210CA I²C support I²C bus Version 2.1 – 2000.

15.1 Features

The following are the features of I²C module:

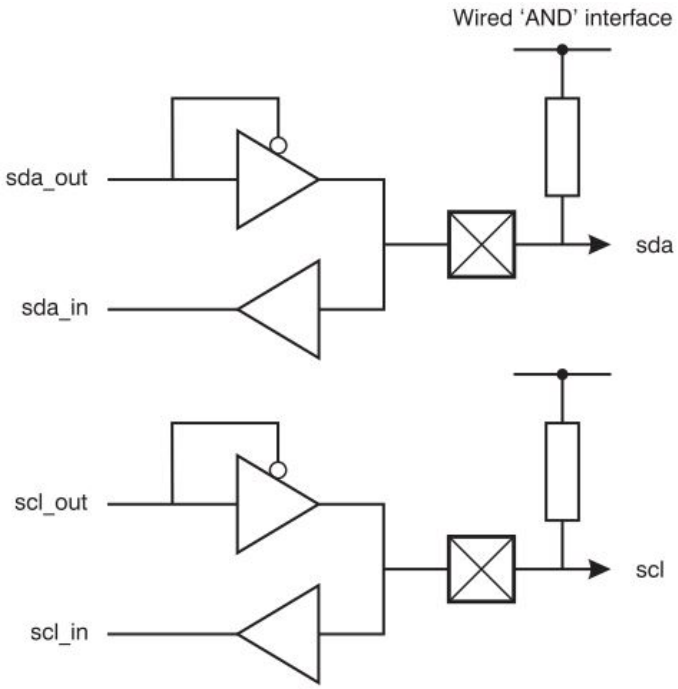
- Two I²C peripherals (I²C0 and I²C1) available
- Modes of operation:
  - Master mode
  - Slave mode
- Clock stretching by slave
- Automatic address recognition in hardware
- Automatic acknowledgment generation
- Standard mode (100 kbps)
- Fast mode (400 kbps)
- High-Speed mode (3.4 Mbps)

15.2 Principal of Operation

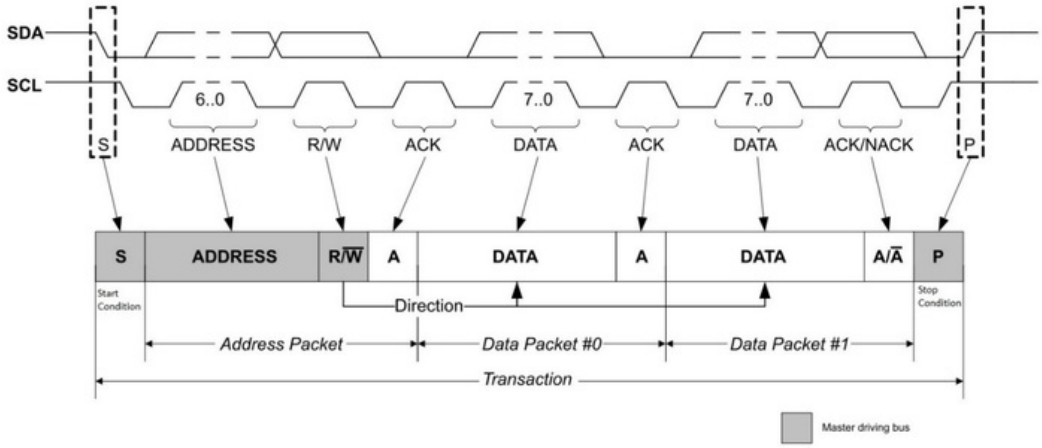
The I²C interface uses two physical lines for communication:

- Serial Data Line (SDA) for packet transfer
- Serial Clock Line (SCL) for the bus clock

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only when the SCL line is low, except for STOP and START conditions. A transaction starts with the I²C master sending the start condition, followed by a 7-bit address and a direction bit (read or write to/from the slave). The addressed I²C slave will then acknowledge (ACK) the address, and data packet transactions can begin. Every 9-bit data packet consists of 8 data bits followed by a one-bit reply indicating whether or not the data was acknowledged. If a data packet is not acknowledged (NACK), whether by the I²C slave or master, the I²C master acts by terminating the transaction by sending the stop condition. The I²C peripheral in ATSAMB11-XR2100A and the ATSAMB11-ZR210CA does not support repeated start and 10-bit slave addressing condition. The output drivers are open-drain to perform wire-AND functions on the bus.



The maximum number of devices on the bus are limited by only the maximum capacitance specification of 400 pF. The following figure illustrates the I²C transaction formats.



The I²C pins SCL and SDA can be selected based on the configuration selected in the Peripheral Multiplexing and MEGAMUXing register. For more details, see Peripheral Multiplexing and MEGAMUXing.

15.3 Clock Configuration

Before configuring the I²C registers, reset the I²C core by setting I2CX_CORE_RSTN bit in LPMCU_GLOBAL_RESET_0 register. Then the clock to the I²C peripheral needs to be enabled. This is done by setting the I2C0_CORE_CLK_EN, I2C1_CORE_CLK_EN bit in LPMCU_CLOCK_ENABLES_0 register for I²C0 and I²C1 respectively. For more details on configuration, see Peripheral Clock Configuration.

15.4 Functional Description

15.4.1 Initialization

- Configure the pin mux register and/or MEGAMUX register (see I/O Peripheral Multiplexing and MegaMuxing) to select the IO pins that need to be used as SCL and SDA lines.
- Select the I^2C module clock source by configuring the CLOCK_SOURCE_SELECT register. The clock sources that can be selected are 26 MHz, 13 MHz, 6.5 MHz and 3 MHz. In Slave mode, the clock source selected should be a factor of at least five times more than the SCL clock from master device. For example, to operate the SCL at 400 kHz a minimum 2 MHz clock is required.
- Set the clock divider value by configuring I2C_CLK_DIVIDER register. In Master mode, the value configured in this register determine the SCL frequency. The clock source selected in CLOCK_SOURCE_SELECT register is divided by (n+1), where n is the value set in I2C_CLK_DIVIDER register.
  SCL Frequency = CLOCK_SOURCE_SELECT/(I2C_CLK_DIVIDER+1)
- To configure the I^2C as master, set the MASTER_ENABLE bit in I2C_MASTER_MODE register.
- To configure the I^2C as slave, write the 7-bit slave address in register I2C_SLAVE_ADDRESS. Clear MASTER_ENABLE bit in I2C_MASTER_MODE register.

15.4.2 Enabling, Disabling, and Flushing

- The I^2C peripheral is enabled by setting the ENABLE bit in I2C_MODULE_ENABLE register. Setting the ENABLE bit enables the I^2C module clock and can perform in I^2C transactions. To generate interrupts on I^2C transaction, the appropriate bits in the interrupt mask registers must be set, as follows:
  - Register the I^2C transmit and receive ISR function
  - Enable the interrupts in NVIC interrupt controller registers. For more details, see Interrupt section.
- The I^2C peripheral is disabled by clearing the ENABLE bit in I2C_MODULE_ENABLE register. If this bit is cleared then the module does not take part in any I^2C transactions and the internal state of the module is reset and placed in a low power mode.
- The I2C_FLUSH register can be used to flush the contents of both the transmit and receive FIFOs. Flushing the transmit FIFO terminates any ongoing transactions when the current byte is transmitted. This allows the software to flush the FIFOs and abort any ongoing transactions.
- The I2C_ACTIVE bit in I2C_STATUS register indicates whether the I^2C peripheral is idle or active state. If the I2C_ACTIVE bit is set, the I^2C module is in active state and the configuration registers should not be changed during this period. If the registers are modified while a transaction is ongoing, the state of the I^2C module cannot be guaranteed.

15.4.3 I^2C Master Operation

- The I^2C transaction is started by setting the ONBUS_ENABLE bit in the I2C_ONBUS register. When operating as a master the module initiates transactions when data are placed in the transmit FIFO, and continues to transmit the content of the FIFO until it is empty. If ONBUS_ENABLE bit is reset to 0 then the module completes the transmission of the current byte and generates a stop condition on the bus.
- The start condition is generated by setting the ADDRESS_FLAG bit in TRANSMIT_DATA register and ONBUS_ENABLE bit in I2C_ONBUS register is enabled. The byte written into the lower 8 [7:1] bits of TRANSMIT_DATA register must then be the address of the device associated with this transaction and the least significant bit 0 of the data indicates the direction of the transaction.

- The NAK bit in RECEIVE_STATUS register is set when a NAK is received. The I²C module automatically retries the transmission, the transaction can be aborted by writing to the I2C_FLUSH register.

15.4.4 I²C Slave Operation

In Slave mode, the NAK bit in RECEIVE_STATUS register is set at the end of a transaction. The module automatically recognizes the end of a transaction and stops; this bit can be used by the software to recognize the end of a transaction.

15.4.5 Transmit and Receive Operation

- The I²C Module has two FIFOs, one for transmit and one for receive to automate transmission/ reception. The data written on TRANSMIT_DATA register pushes one byte into the transmit FIFO.
- The TRANSMIT_STATUS register reflects the state of the I²C transmitter. If the corresponding bits are set in the TX_INTERRUPT_MASK register then interrupts can be generated upon the bit in this register being set. To enable the I²C interrupt on transmit, register the I²C transmit ISR function and enable the interrupts in NVIC interrupt controller registers. For more details, see Interrupt.
- Reading from the RECEIVE_DATA register pops one byte from the receive FIFO.
- The RECEIVE_STATUS register reflects the state of the I²C receiver. If the corresponding bits are set in the RX_INTERRUPT_MASK mask register, then interrupts can be generated upon the bit in this register being set. To enable the I²C interrupt on reception, register the I²C receive ISR function and enable the interrupts in NVIC interrupt controller registers. For more details, see Interrupt.

15.5 Power Management

If the system goes to the Ultra-Low Power mode, the I²C peripheral shuts down. The I²C configuration registers lose their content, and are not restored when powered- up again. User must reconfigure the I²C peripheral at power-up to ensure it is in a well-defined state before use. For details on reconfiguration, refer to ATSAMB11 BluSDK Smart Interrupts and ULP Architecture and Usage User Guide. This document also explains on how sleep and wake-up are controlled.

15.6 Register Summary

This is the summary of all the registers used in this chapter.

Absolute Address	Register Group	Name	Bit Pos.								
0x40003000	I2C0 Register	TRANSMIT_DATA	7:0	TX_DATA[7:0]							
0x40003400	I2C1 Register		15:8								ADDRESS_FLAG
0x40003004	I2C0 Register	RECEIVE_DATA	7:0	RX_BYTE[7:0]							
0x40003404	I2C1 Register										
0x40003008	I2C0 Register	TRANSMIT_STATUS	7:0				TX_FIFO_EMPTY	TX_FIFO_0P75_EMPTY	TX_FIFO_0P5_EMPTY	TX_FIFO_0P25_EMPTY	TX_FIFO_NOT_FULL
0x40003408	I2C1 Register										
0x4000300C	I2C0 Register	RECEIVE_STATUS	7:0			NAK	FIFO_OVERRUN	RX_FIFO_0P75_FULL	RX_FIFO_0P5_FULL	RX_FIFO_0P25_FULL	RX_FIFO_NOT_EMPTY
0x4000340C	I2C1 Register										
0x40003010	I2C0 Register	CLOCK_SOURCE_SELECT	7:0							CLOCK[1:0]	
0x40003410	I2C1 Register										
0x40003014	I2C0 Register	I2C_MODULE_ENABLE	7:0								ENABLE
0x40003414	I2C1 Register										

Absolute Address	Register Group	Name	Bit Pos.								
0x40003018	I2C0 Register	I2C_CLK_DIVIDER	7:0	I2C_DIVIDE_RATIO[7:0]							
0x40003418	I2C1 Register		15:8	I2C_DIVIDE_RATIO[15:8]							
0x4000301C	I2C0 Register	I2C_MASTER_MODE	7:0								MASTER_ENABLE
0x4000341C	I2C1 Register										
0x40003020	I2C0 Register	I2C_ONBUS	7:0								ONBUS_ENABLE
0x40003420	I2C1 Register										
0x40003024	I2C0 Register	I2C_SLAVE_ADDRESS	7:0	ADDRESS[6:0]							
0x40003424	I2C1 Register										
0x40003028	I2C0 Register	I2C_STATUS	7:0								I2C_ACTIVE
0x40003428	I2C1 Register										
0x4000302C	I2C0 Register	TX_INTERRUPT_MASK	7:0				TX_FIFO_EMPTY_MASK	TX_FIFO_0P75_EMPTY_MASK	TX_FIFO_0P5_EMPTY_MASK	TX_FIFO_0P25_EMPTY_MASK	TX_FIFO_NOT_FULL_MASK
0x4000342C	I2C1 Register										
0x40003030	I2C0 Register	RX_INTERRUPT_MASK	7:0			NAK_MASK	FIFO_OVERRUN_MASK	RX_FIFO_0P75_FULL_MASK	RX_FIFO_0P5_FULL_MASK	RX_FIFO_0P25_FULL_MASK	RX_FIFO_NOT_EMPTY_MASK
0x40003430	I2C1 Register										
0x40003034	I2C0 Register	I2C_FLUSH	7:0								I2C_FLUSH
0x40003434	I2C1 Register										
0x4000B044	LPMCU_MISC_REGS0	PINMUX_SEL_0	7:0	PINMUX_SEL[2:0] LP_GPIO_1					PINMUX_SEL[2:0] LP_GPIO_0		
			15:8	PINMUX_SEL[2:0] LP_GPIO_3					PINMUX_SEL[2:0] LP_GPIO_2		
			23:16	PINMUX_SEL[2:0] LP_GPIO_5					PINMUX_SEL[2:0] LP_GPIO_4		
			31:24	PINMUX_SEL[2:0] LP_GPIO_7					PINMUX_SEL[2:0] LP_GPIO_6		
0x4000B048	LPMCU_MISC_REGS0	PINMUX_SEL_1	7:0	PINMUX_SEL[2:0] LP_GPIO_9					PINMUX_SEL[2:0] LP_GPIO_8		
			15:8	PINMUX_SEL[2:0] LP_GPIO_11					PINMUX_SEL[2:0] LP_GPIO_10		
			23:16	PINMUX_SEL[2:0] LP_GPIO_13					PINMUX_SEL[2:0] LP_GPIO_12		
			31:24	PINMUX_SEL[2:0] LP_GPIO_15					PINMUX_SEL[2:0] LP_GPIO_14		
0x4000B04C	LPMCU_MISC_REGS0	PINMUX_SEL_2	7:0	PINMUX_SEL[2:0] LP_GPIO_17					PINMUX_SEL[2:0] LP_GPIO_16		
			15:8	PINMUX_SEL[2:0] LP_GPIO_19					PINMUX_SEL[2:0] LP_GPIO_18		
			23:16	PINMUX_SEL[2:0] LP_GPIO_21					PINMUX_SEL[2:0] LP_GPIO_20		
			31:24	PINMUX_SEL[2:0] LP_GPIO_23					PINMUX_SEL[2:0] LP_GPIO_22		
0x4000B080	LPMCU_MISC_REGS0	PINMUX_SEL_4	7:0						PINMUX_SEL[2:0] LP_GPIO_24		
			15:8								
			23:16								
			31:24								
0x4000B1A0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_0	7:0	MEGAMUX_SEL[5:0] LP_GPIO_0							
			15:8	MEGAMUX_SEL[5:0] LP_GPIO_1							
			23:16	MEGAMUX_SEL[5:0] LP_GPIO_2							
			31:24	MEGAMUX_SEL[5:0] LP_GPIO_3							
0x4000B1A4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_1	7:0	MEGAMUX_SEL[5:0] LP_GPIO_4							
			15:8	MEGAMUX_SEL[5:0] LP_GPIO_5							
			23:16	MEGAMUX_SEL[5:0] LP_GPIO_6							
			31:24	MEGAMUX_SEL[5:0] LP_GPIO_7							
0x4000B1A8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_2	7:0	MEGAMUX_SEL[5:0] LP_GPIO_8							
			15:8	MEGAMUX_SEL[5:0] LP_GPIO_9							
			23:16	MEGAMUX_SEL[5:0] LP_GPIO_10							
			31:24	MEGAMUX_SEL[5:0] LP_GPIO_11							

Absolute Address	Register Group	Name	Bit Pos.								
0x4000B1AC	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_3	7:0			MEGAMUX_SEL[5:0] LP_GPIO_12					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_13					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_14					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_15					
0x4000B1B0	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_4	7:0			MEGAMUX_SEL[5:0] LP_GPIO_16					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_17					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_18					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_19					
0x4000B1B4	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_5	7:0			MEGAMUX_SEL[5:0] LP_GPIO_20					
			15:8			MEGAMUX_SEL[5:0] LP_GPIO_21					
			23:16			MEGAMUX_SEL[5:0] LP_GPIO_22					
			31:24			MEGAMUX_SEL[5:0] LP_GPIO_23					
0x4000B1B8	LPMCU_MISC_REGS0	MEGA_MUX_IO_SEL_6	7:0			MEGAMUX_SEL[5:0] LP_GPIO_24					
0x4000B0C0	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_0	7:0				MUX_0[4:0]				
			15:8				MUX_1[4:0]				
			23:16				MUX_2[4:0]				
			31:24				MUX_3[4:0]				
0x4000B0C4	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_1	7:0				MUX_4[4:0]				
			15:8				MUX_5[4:0]				
			23:16				MUX_6[4:0]				
			31:24				MUX_7[4:0]				
0x4000B0C8	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_2	7:0				MUX_8[4:0]				
			15:8				MUX_9[4:0]				
			23:16				MUX_10[4:0]				
			31:24				MUX_11[4:0]				
0x4000B0CC	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_3	7:0				MUX_12[4:0]				
			15:8				MUX_13[4:0]				
			23:16				MUX_14[4:0]				
			31:24				MUX_15[4:0]				
0x4000B0D0	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_4	7:0				MUX_16[4:0]				
			15:8				MUX_17[4:0]				
			23:16				MUX_18[4:0]				
			31:24				MUX_19[4:0]				
0x4000B0D4	LPMCU_MISC_REGS0	IRQ_MUX_IO_SEL_5	7:0				MUX_20[4:0]				

15.7 Register Description

15.7.1 I2C Transmit Data

Name: TRANSMIT_DATA
Reset: 0x0000

Absolute Address: 0x40003000 (I2C0), 0x40003400 (I2C1)

This register is a part of I2C Registers. Writing this register pushes one byte of data into the transmit FIFO of I2C module.

Bit	15	14	13	12	11	10	9	8
								ADDRESS_FLAG
Access								W
Reset								0

Bit	7	6	5	4	3	2	1	0
	TX DATA[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit 8 – ADDRESS_FLAG
Writing '1' to bit indicate the start of I2C transaction. When this bit is set, the byte written into the lower 8 bits of this register should then be the address of the device associated with this transaction. When this bit is set the least significant bit of the data is used to indicate the direction of the transaction.

ADDRESS_FLAG	TX_DATA
0	Bits 7:0 is data
1	Bits 7:1 is Address of the slave Bit 0: Direction of Transaction

Bits 7:0 – TX DATA[7:0]
These eight bits are the data or address to transmit (see ADDRESS_FLAG table).

Writing '0' to Bit 0, indicates the write command and the direction is writing to slave from master.

Writing '1' to Bit 0, indicates the read command and the direction is reading from slave by master.

15.7.2 I2C Receive Data

Name: RECEIVE_DATA
Reset: 0x00

Absolute Address: 0x40003004 (I2C0), 0x40003404 (I2C1)

This register is a part of I2C Registers. Reading this register pops one byte of received data from receive FIFO.

Bit	7	6	5	4	3	2	1	0
	RX_BYTE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RX_BYTE[7:0]
Reading from this 8-bit read only register pops one byte from the receive FIFO.

15.7.3 I2C Transmit Status

Name: TRANSMIT_STATUS
Reset: 0x1F

Absolute Address: 0x40003008 (I2C0), 0x40003408 (I2C1)

This register is a part of I2C Registers. This register provides the status of I2C transmit operation.

Bit	7	6	5	4	3	2	1	0
				TX_FIFO_EMPTY	TX_FIFO_0P75_EMPTY	TX_FIFO_0P5_EMPTY	TX_FIFO_0P25_EMPTY	TX_FIFO_NOT_FULL
Access				R	R	R	R	R
Reset				1	1	1	1	1

Bit 4 – TX_FIFO_EMPTY
This bit is set if the FIFO is completely empty.

Bit 3 – TX_FIFO_0P75_EMPTY
This bit is set if the FIFO is three-quarters empty.

Bit 2 – TX_FIFO_0P5_EMPTY
This bit is set if the FIFO is half empty.

Bit 1 – TX_FIFO_0P25_EMPTY
This bit is set if the FIFO is one quarter empty.

Bit 0 – TX_FIFO_NOT_FULL
This bit is set if there is at least space for one more byte in the FIFO.
Reading '0' indicates TX FIFO is full.

15.7.4 I2C Receive Status

Name: RECEIVE_STATUS
Reset: 0x00

Absolute Address: 0x4000300C (I2C0), 0x4000340C (I2C1)

This register is a part of I2C Registers. This register provides the status of I2C transmit operation.

Bit	7	6	5	4	3	2	1	0
			NAK	FIFO_OVERRUN	RX_FIFO_0P75_FULL	RX_FIFO_0P5_FULL	RX_FIFO_0P25_FULL	RX_FIFO_NOT_EMPTY
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 5 – NAK
This bit is set when NAK is received. The I2C module retries transmission unless transaction aborted by the flush register. This bit is reset after the status register is read.

Bit 4 – FIFO_OVERRUN
This bit is set when a character is received but there is no place left in the FIFO to store it.

This bit is reset after the status register is read.

Bit 3 – RX_FIFO_0P75_FULL
This bit is set if the FIFO is three-quarters full.

Bit 2 – RX_FIFO_0P5_FULL
This bit is set if the FIFO is half full.

Bit 1 – RX_FIFO_0P25_FULL
This bit is set if the FIFO is one quarter full.

Bit 0 – RX_FIFO_NOT_EMPTY
This bit is set if there is at least space for one more byte in the FIFO.
Reading '0' indicates RX FIFO is Empty.

15.7.5 I2C Clock Source Select

Name: CLOCK_SOURCE_SELECT
Reset: 0x00

Absolute Address: 0x40003010 (I2C0), 0x40003410 (I2C1)

This register is a part of I2C Registers. This register allows the user to select the input clock source for I2C peripheral.

Bit	7	6	5	4	3	2	1	0
							CLOCK[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – CLOCK[1:0]
Selects the input clock for I2C module.

CLOCK[1:0]	Description
0	26 MHz clock
1	13 MHz clock
2	6.5 MHz clock
3	3.25 MHz clock

15.7.6 I2C Module Enable

Name: I2C_MODULE_ENABLE
Reset: 0x00

Absolute Address: 0x40003014 (I2C0), 0x40003414 (I2C1)

This register is a part of I2C Registers. This register allows the user to enable/disable the I2C peripheral.

Bit	7	6	5	4	3	2	1	0
								ENABLE
Access								R/W
Reset								0

Bit 0 – ENABLE
Writing '0' to this bit disables I2C module
Writing '1' to this bit enables I2C module.

15.7.7 I2C SCK Clock Divider

Name: I2C_CLK_DIVIDER
Reset: 0x0000

Absolute Address: 0x40003018 (I2C0), 0x40003418 (I2C1)

This register is a part of I2C Registers. This register sets the divide ratio used to generate the SCK clock from the module's input clock.

Bit	15	14	13	12	11	10	9	8
	I2C_DIVIDE_RATIO[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	I2C_DIVIDE_RATIO[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – I2C_DIVIDE_RATIO[15:0]
Sets the divide ratio used to generate the SCK clock signal from the clock selected by the CLOCK_SOURCE_SELECT register. The minimum division is by 2; a value of 0 is not valid.

SCK Clock = CLOCK[1:0] / (I2C_DIVIDE_RATIO[15:0]+1)

15.7.8 I2C Master Mode Enable

Name: I2C_MASTER_MODE
Reset: 0x00

Absolute Address: 0x4000301C (I2C0), 0x4000341C (I2C1)

This register allows the user to select I2C between Master and Slave modes.

Bit	7	6	5	4	3	2	1	0
								MASTER_ENABLE
Access								R/W
Reset								0

Bit 0 – MASTER_ENABLE
Writing '0' to this bit enables I2C in Slave mode.

Writing '1' to this bit enables I2C in Master mode.

15.7.9 I2C Start Master Transaction

Name: I2C_ONBUS
Reset: 0x00

Absolute Address: 0x40003020 (I2C0), 0x40003420 (I2C1)

This register is a part of I2C Registers. This register initiates the I2C transactions when in Master mode.

Bit	7	6	5	4	3	2	1	0
								ONBUS_ENABLE
Access								R/W
Reset								0

Bit 0 – ONBUS_ENABLE
Active High Enable to initiate transactions when in Master mode

Writing '0' to this bit Master completes current byte and generates stop condition on bus

Writing '1' to this bit Master transmits contents of FIFO until empty

15.7.10 I2C Slave Address

Name: I2C_SLAVE_ADDRESS
Reset: 0x00

Absolute Address: 0x40003024 (I2C0), 0x40003424 (I2C1)

This register is a part of I2C Registers. This seven bit read/write register sets the I2C slave address.

Bit	7	6	5	4	3	2	1	0
		ADDRESS[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:0 – ADDRESS[6:0]
These bits hold the I2C slave address.

15.7.11 I2C Status

Name: I2C_STATUS
Reset: 0x00

Absolute Address: 0x40003028 (I2C0), 0x40003428 (I2C1)

This register is a part of I2C Registers.

Bit	7	6	5	4	3	2	1	0
								I2C_ACTIVE
Access								R
Reset								0

Bit 0 – I2C_ACTIVE
The I2C configuration registers must not be changed when this bit is set. If the registers are modified during transaction is ongoing, the state of the I2C module is not guaranteed.

Read Value	Description
0	I2C is idle
1	I2C is active

15.7.12 I2C Transmit Interrupt Mask

Name: TX_INTERRUPT_MASK
Reset: 0x00

Absolute Address: 0x4000302C (I2C0), 0x4000342C (I2C1)

This register is a part of I2C Registers. This register is used to enable or disable the generation of I2C transmission interrupts. During the I2C transmission interrupt, if a bit in TX_INTERRUPT_MASK register is set and its corresponding bit in TRANSMIT_STATUS register is set then an interrupt is generated.

Bit	7	6	5	4	3	2	1	0
				TX_FIFO_EMPTY_MASK	TX_FIFO_0P75_EMPTY_MASK	TX_FIFO_0P5_EMPTY_MASK	TX_FIFO_0P25_EMPTY_MASK	TX_FIFO_NOT_FULL_MASK
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	0	0	0	0

Bit 4 – TX_FIFO_EMPTY_MASK
Writing '0' disables the TX_FIFO_EMPTY interrupt.
Writing '1' enables the TX_FIFO_EMPTY interrupt.

Bit 3 – TX_FIFO_0P75_EMPTY_MASK
Writing '0' disables the TX_FIFO_0P75_EMPTY interrupt.
Writing '1' enables the TX_FIFO_0P75_EMPTY interrupt.

Bit 2 – TX_FIFO_0P5_EMPTY_MASK
Writing '0' disables the TX_FIFO_0P5_EMPTY interrupt.
Writing '1' enables the TX_FIFO_0P5_EMPTY interrupt.

Bit 1 – TX_FIFO_0P25_EMPTY_MASK
Writing '0' disables the TX_FIFO_0P25_EMPTY interrupt.
Writing '1' enables the TX_FIFO_0P25_EMPTY interrupt.

Bit 0 – TX_FIFO_NOT_FULL_MASK
Writing '0' disables the TX_FIFO_NOT_FULL interrupt.
Writing '1' enables the TX_FIFO_NOT_FULL interrupt.

15.7.13 I2C Receive Interrupt Mask

Name: RX_INTERRUPT_MASK
Reset: 0x00

Absolute Address: 0x40003030 (I2C0), 0x40003430 (I2C1)

This register is a part of I2C Registers. This register is used to enable or disable the generation of I2C receive interrupts. During the I2C receive interrupt, if a bit in RX_INTERRUPT_MASK register is set and its corresponding bit in RECEIVE_STATUS register is set then an interrupt is generated.

Bit	7	6	5	4	3	2	1	0
			NAK_MASK	FIFO_OVERRUN_MASK	RX_FIFO_0P75_FULL_MASK	RX_FIFO_0P5_FULL_MASK	RX_FIFO_0P25_FULL_MASK	RX_FIFO_NOT_EMPTY_MASK
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 5 – NAK_MASK
Writing '0' disables the NAK interrupt.
Writing '1' enables the NAK interrupt.

Bit 4 – FIFO_OVERRUN_MASK
Writing '0' disables the FIFO_OVERRUN interrupt.
Writing '1' enables the FIFO_OVERRUN interrupt.

Bit 3 – RX_FIFO_0P75_FULL_MASK
Writing '0' disables the RX_FIFO_0P75_FULL interrupt.
Writing '1' enables the RX_FIFO_0P75_FULL interrupt.

Bit 2 – RX_FIFO_0P5_FULL_MASK
Writing '0' disables the RX_FIFO_0P5_FULL interrupt.
Writing '1' enables the RX_FIFO_0P5_FULL interrupt.

Bit 1 – RX_FIFO_0P25_FULL_MASK
Writing '0' disables the RX_FIFO_0P25_FULL interrupt.
Writing '1' enables the RX_FIFO_0P25_FULL interrupt.

Bit 0 – RX_FIFO_NOT_EMPTY_MASK
Writing '0' disables the RX_FIFO_NOT_EMPTY interrupt.
Writing '1' enables the RX_FIFO_NOT_EMPTY interrupt.

15.7.14 I2C FLUSH

Name: I2C_FLUSH
Reset: 0x00

Absolute Address: 0x40003034 (I2C0), 0x40003434 (I2C1)

This register is a part of I2C Registers. This register allows the software to flush the FIFOs and abort any ongoing transactions.

Bit	7	6	5	4	3	2	1	0
								I2C_FLUSH
Access								W
Reset								0

Bit 0 – I2C_FLUSH
Writing to this address flushes the content of both the Tx and Rx FIFOs. The written value does not have effect. Flushing the Tx FIFO aborts the ongoing transactions when the current byte is being transmitted.

16. Peripherals

16.1 Timer

The 32-bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation, and time tracking.

Note: ARM Timer is one of the reserved resources being used by the BLE stack. Application must refrain from using this peripheral.

16.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in a Free-running, Periodic, or One-shot mode.

16.3 Watchdog Timer

The two watchdog blocks allow the CPU to be interrupted, if it has not interacted with the watchdog timer before it expires. In addition, this interrupt will be an output of the core, so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This will allow the CPU to get back to a known state in the event, a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

Watchdog timer 0 is a reserved resource, being used by the BLE stack. Application must refrain from using the watchdog timer 0.

16.4 SPI Controller

16.4.1 SPI Master/Slave Interface

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA provides a Serial Peripheral Interface (SPI) that can be configured as master or slave. The SPI Interface pins are mapped, as illustrated in the following table. The SPI Interface is a full-duplex slave-synchronous serial interface. When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line. The SPI slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

Table 16-1. SPI Interface Pin Mapping

Pin Name	SPI Function
SSN	Active-Low Slave Select
SCK	Serial Clock
MOSI	Master Out Slave In (Data)
MISO	Master In Slave Out (Data)

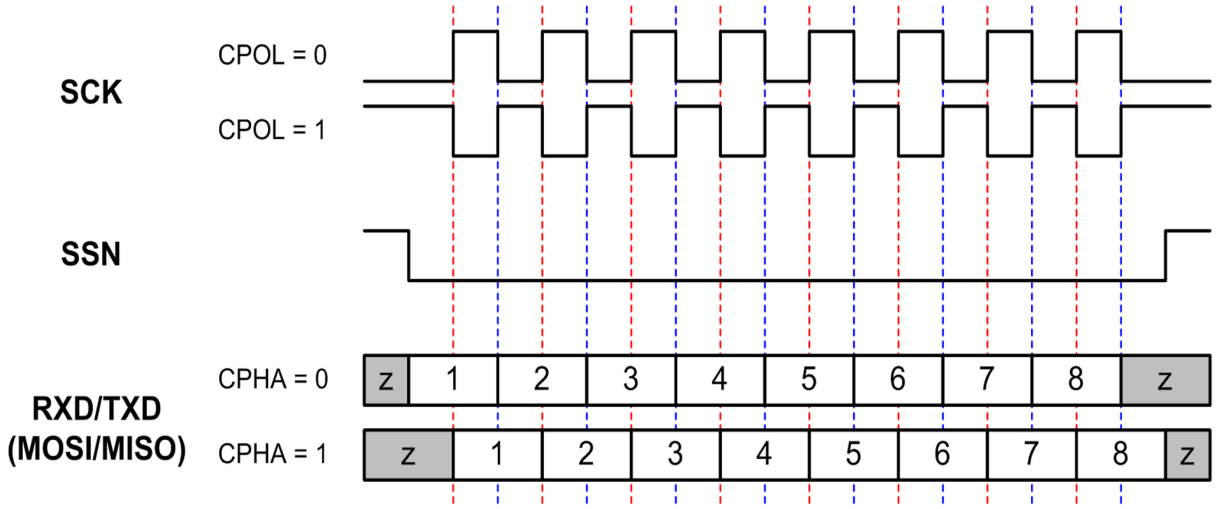
16.4.1.1 SPI Interface Modes

The SPI Interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 16-2 and Figure 16-1. The red lines in Figure 16-1 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 16-2. SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 16-1. SPI Clock Polarity and Clock Phase Timing



16.5 SPI-Flash Controller

The AHB SPI-Flash Controller is used to access the internal stacked SPI Flash to access various instruction/data code required for storing application code, code patches, and OTA images. It supports several SPI modes including 0, 1, 2, and 3.

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA provide an SPI Master interface for accessing the internal stacked SPI Flash memory. The TXD pin is same as the Master Output, Slave Input (MOSI), and the RXD pin is the same as the Master Input, Slave Output (MISO). The SPI Master interface supports all four standard modes of clock polarity and clock phase, as shown in Table 16-2. Internal stacked SPI Flash memory is accessed by a processor programming commands to the SPI Master interface, which in turn initiates SPI master access to the Flash.

16.6 UART Interface

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA provide Universal Asynchronous Receiver/ Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem contains two UART interfaces: 2-pin mode for data only, and a 4-pin interface for flow control and data transfer. The UART

interfaces are compatible with the RS-232 standard, where the ATSAMB11-XR2100A and ATSAMB11-ZR210CA operate as Data Terminal Equipment (DTE). The 4-pin UART has two pins for data (TX and RX) and two pins for flow control/handshaking: Request To Send (RTS) and Clear To Send (CTS).

⚠ CAUTION The RTS and CTS are used for hardware flow control. The RTS and CTS pins must be interfaced to the remote device and hardware flow control must be enabled to guarantee data integrity.

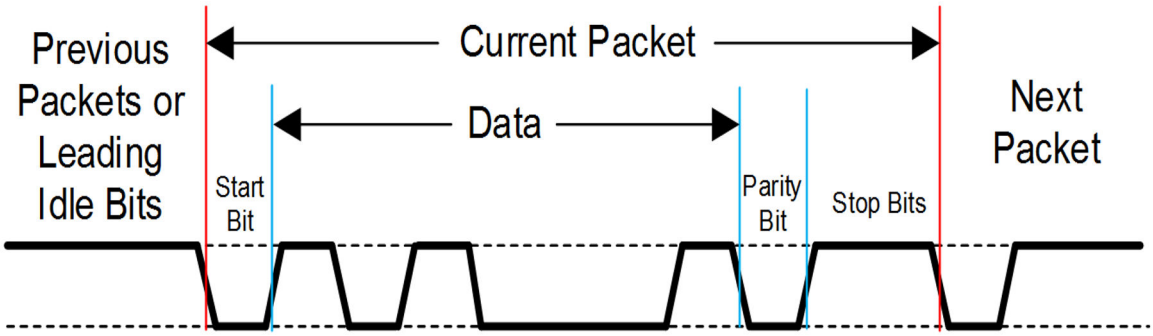
The pins associated with each UART interfaces can be enabled on several alternative pins by programming their corresponding pin-MUX control registers (see I/O Port Function Multiplexing and MEGAMUX Options for available options).

The UART features the programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 26 MHz, 13 MHz, 6.5 MHz, and 3.25 MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 26 MHz/8.0 = 3.25 MBd.

The UART can be configured for 7- or 8-bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also contains RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also contains status registers showing the number of received characters available in the FIFO and various error conditions, and also the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 16-2. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 16-2. Example of UART RX or TX Packet



16.7 DMA Controller

Direct Memory Access (DMA) allows certain hardware subsystems to access main system memory independent of the Cortex-M0 Processor.

The DMA features and benefits are:

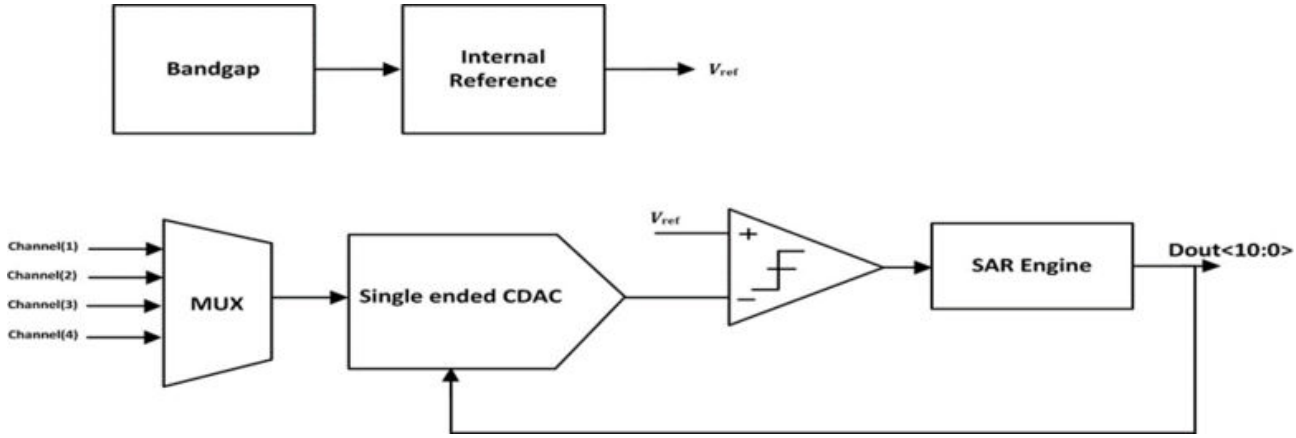
- Supports any address alignment

- Supports any buffer size alignment
- Peripheral flow control and peripheral block transfer
- The following modes are supported:
  - Peripheral to peripheral transfer
  - Memory to memory
  - Memory to peripheral
  - Peripheral to memory
  - Register to memory
- Interrupts for both TX done and RX done in memory and peripheral mode
- Scheduled transfers
- Endianness byte swapping
- Watchdog timer
- 4-channel operation
- 32-bit Data width
- AHB MUX (on read and write buses)
- Command lists support
- Usage of tokens

16.8 Analog to Digital Converter

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have an integrated Successive Approximation Register (SAR) ADC with 11-bit resolution and variable conversion speed up 1MS/s. The key building blocks are the capacitive DAC, comparator, and synchronous SAR engine as illustrated in the following figure.

Figure 16-3. SAR ADC Block Diagram



The ADC reference voltage can be either generated internally or set externally via one of the four available Mixed Signal GPIO pins on the ATSAMB11-XR2100A and the ATSAMB11-ZR210CA.

There are two modes of operation:

- High resolution (11-bit): Set the reference voltage to half the supply voltage or below. In this condition the input signal dynamic range is equal to twice the reference voltage (ENOB=10-bit).

- Medium Resolution (10-bit) : Set the reference voltage to any value below supply voltage (up to supply voltage - 300 mV) and in this condition the input dynamic range is from zero to the reference voltage (ENOB = 9-bit).

Four input channels are time multiplexed to the input of the SAR ADC. However, on the ATSAMB11, only four channel inputs are accessible from the outside, through the Mixed Signal GPIO pin numbers listed in I/O Port Function Multiplexing.

In Power-Saving mode, the internal reference voltage is completely off and the reference voltage is set externally.

The ADC characteristics are summarized in the following table.

Table 16-3. SAR ADC Characteristics

Conversion rate	1 ks → 1 MS
Selectable Resolution	10 → 11 bit
Power consumption	13.5 µA (at 100 KS/s) (1)

Note:

1. With external reference.

16.8.1 Timing

The ADC timing is shown in Figure SAR ADC Timing. The input signal is sampled twice, in the first sampling cycle the input range is defined either to be above reference voltage or below it and in the second sampling instant the ADC start its normal operation.

The ADC takes two sampling instants and N-1 conversion cycle (N=ADC resolution) and one cycle to sample the data out. Therefore, for the 11-bit resolution, it takes 13 clock cycles to do one Sample conversion.

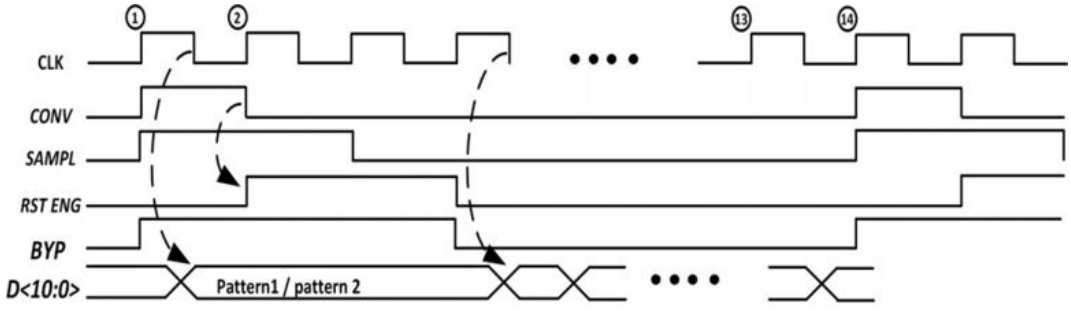
The Input clock equals N+2 the sampling clock frequency (N is the ADC resolution).

CONV signal : Gives indication about end of conversion.

SAMPL : The input signal is sampled when this signal is high.

RST ENG : When High SAR Engine is in reset mode (SAR engine output is set to mid-scale).

Figure 16-4. SAR ADC Timing



16.9 Three-axis Quadrature Decoder

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have a three-axis Quadrature decoder (X, Y, and Z) that can determine the direction and speed of movement on three axes, requiring in total six GPIO pins to

interface with the sensors. The sensors are expected to provide pulse trains as inputs to the quadrature decoder.

Each axis channel input will have two pulses with ±90 degrees phase shift depending on the direction of movement. The decoder counts the edges of the two waveforms to determine the speed and uses the phase relationship between the two inputs to determine the direction of motion.

The decoder is configured to interrupt ARM based on independent thresholds for each direction. Each quadrature clock counter (X, Y, and Z) is an unsigned 16-bit counter and the system clock uses a programmable sampling clock ranging from 26 MHz, 13, 6.5, to 3.25 MHz.

If wakeup is desired from threshold detection on an axis input, AO_GPIO_0 needs to be used.

16.10 Clock Output

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA have an option to output a clock. The clock can be output to any GPIO pin via the test MUX. Note that this feature requires that the ARM and BLE power domains stay on. If BLE is not used, the clocks to the BLE core are gated off, resulting in small leakage. The following two methods can be used to output a clock.

Note: Refer the BluSDK Smart BLE API Software Development Guide for details on how to enable the 32.768 kHz clock output.

16.10.1 Variable Frequency Clock Output Using Fractional Divider

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA can output the variable frequency ADC clock using a fractional divider of the 26 MHz oscillator. This clock needs to be enabled using bit 10 of the lpmcu_clock_enables_1 register. The clock frequency can be controlled by the divider ratio using the sens_adc_clk_ctrl register (12-bits integer part, 8-bit fractional part).The division ratio can vary from 2 to 4096 delivering output frequency between 6.35 kHz to 13 MHz. This is a digital divider with pulse swallowing implementation, so the clock edges may not be at exact intervals for the fractional ratios. However, it is exact for integer division ratios.

16.10.2 Fixed Frequency Clock Output

The ATSAMB11-XR2100A and ATSAMB11-ZR210CA can output the following fixed-frequency clocks:

- 52 MHz derived from XO
- 26 MHz derived from XO
- 32.768 kHz derived from the RTC XO
- 26 MHz derived from 26 MHz RC Osc.
- 6.5 MHz derived from XO
- 3.25 MHz derived from 26 MHz RC Osc.

For clocks with frequency of 26 MHz and above, ensure that external pad load on the board is minimized to get a clean waveform.

17. Electrical Characteristics

There are voltage ranges where different VDDIO levels apply. This separation is for the IO drivers whose drive strength is directly proportional to the IO supply voltage. In the ATSAMB11 products, there is a large gap in the IO supply voltage range (2.3V to 3.6V). A guarantee on drive strength across this voltage range would be intolerable to most vendors who only use a subsection of the IO supply range. As such, these voltages are segmented into two manageable sections referenced as VDDIOM, and VDDIOH in tables listed in this document..

17.1 Absolute Maximum Ratings

The values listed in this section are ratings that can be peaked by the device, but not sustained without causing irreparable damage to the device.

Table 17-1. Absolute Maximum Ratings

Symbol	Characteristics	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	4.2	V
VBAT	Battery Supply Voltage	-0.3	5.0	
V_{IN} (1)	Digital Input Voltage	-0.3	VDDIO	
V_{AIN} (2)	Analog Input Voltage	-0.3	1.5	
T_A	Storage Temperature	-65	150	°C

Note:

1. V_{IN} corresponds to all the digital pins.
2. V_{AIN} corresponds to all the analog pins, RFIO, XO_N, XO_P, TPP, RTC_CLK_N and RTC_CLK_P.

17.2 Recommended Operating Conditions

Table 17-2. Recommended Operating Conditions

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_M$	I/O Supply Voltage Mid-Range	2.3	2.50	3.00	V
$VDDIO_H$	I/O Supply Voltage High Range	3.00	3.30	3.60	
VBAT	Battery Supply Voltage (1)	2.3	3.6	4.3	
	Operating Temperature	-40		85	°C

Note:

1. VBAT must not be less than VDDIO.

17.3 DC Characteristics

The Table 17-3 provides the DC characteristics for the digital pads.

Table 17-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_M$	Input Low Voltage V_{IL}	-0.30		0.63	V
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
$VDDIO_H$	Input Low Voltage V_{IL}	-0.30		0.65	
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
All	Output Loading			20	pF
	Digital Input Load			6	
$VDDIO_M$	Pad drive strength (regular pads (1))	3.4	6.6		mA
$VDDIO_H$	Pad drive strength (regular pads (1))	10.5	14		
$VDDIO_M$	Pad drive strength (high-drive pads (1))	6.8	13.2		
$VDDIO_H$	Pad drive strength (high-drive pads (1))	21	28		

Note:

1. The following GPIO pads are high-drive pads: GPIO_8, GPIO_9; all other pads are regular pads.

17.4 Receiver Performance

Table 17-4. BLE Receiver Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Sensitivity with on-chip DC/DC(1)	-92.7	-91.9		dBm
Maximum receive signal level		+5		
CCI		12.5		dB
ACI (N±1)		0		

Parameter	Minimum	Typical	Maximum	Unit
N+2 Blocker (Image)		-20		
N-2 Blocker		-38		
N+3 Blocker (Adj. Image)		-35		
N-3 Blocker		-43		
N±4 or greater		-45		dB
Intermod (N+3, N+6)		-32		dBm
OOB (2 GHz<f<2.399 GHz)	-15			
OOB (f<2 GHz or f>2.5 GHz)	-10			

All measurements are taken after the RF input matching network. Refer to the reference schematic of Figure 19-1.

All measurements are performed at VBAT - 3.3V; VDDIO-3.3V and 25°C, with tests following the Bluetooth V4.2 standard tests.

Note:

1. Typical receiver sensitivity is average across 40 channels.

17.5 Transmitter Performance

The transmitter contains fine step power control with P_{out} variable in <3 dB steps below 0 dBm and in <0.5 dB steps above 0 dBm.

Table 17-5. BLE Transmitter Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Maximum output power		3.5		dBm
In-band Spurious (N±2)		-45		
In-band Spurious (N±3)		-50		
2nd harmonic P_{out}	-41			
3rd harmonic P_{out}	-41			
4th harmonic P_{out}	-41			
5th harmonic P_{out}	-41			
Frequency deviation		±250		kHz

All measurements are taken after the RF input matching network. Refer to the reference schematic Figure 19-1.

All measurements are performed at VBAT - 3.3V; VDDIO - 3.3V and 25°C, with tests following the Bluetooth V4.2 standard tests.

Note:

1. At 0 dBm TX output power.
2. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
3. Country specific settings (as per the Module Certifications) should be programmed at the Host product factory to match the intended Destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

17.6 Current Consumption in Various Device States

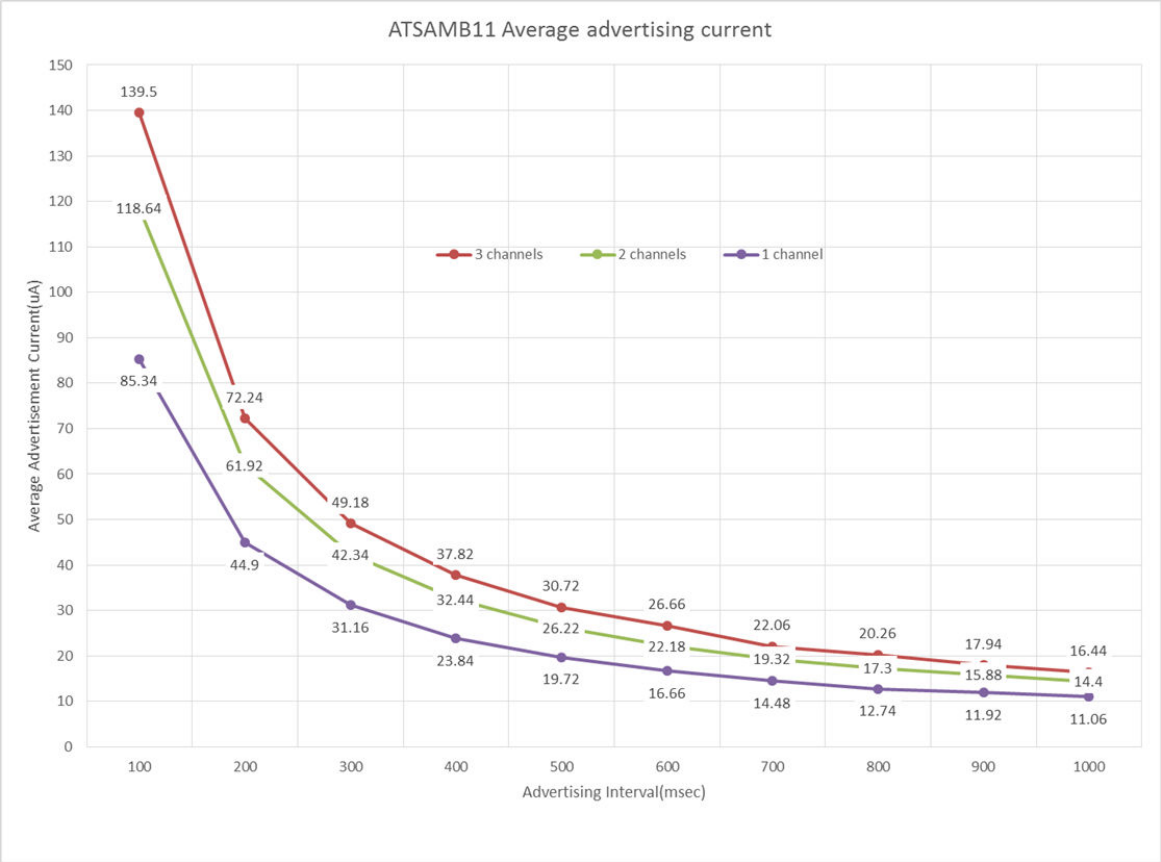
Table 17-6. Device State Current Consumption

Device State	C_EN	VDDIO	I_{VBAT}+I_{VDDIO} (typical) (2)
Power_Down	Off	On	0.03 µA
Ultra_Low_Power with BLE timer, with RTC (1)	On	On	2.03 µA
MCU_Only, idle	On	On	1.35 mA
BLE_On_Receive @channel 37 (2402 MHz)	On	On	5.26 mA
BLE_On_Transmit, 0 dBm output power @Channel 37 (2402 MHz)	On	On	4.18 mA
BLE_On_Transmit, 0 dBm output power @Channel 39 (2480 MHz)	On	On	3.71 mA
BLE_On_Transmit, 3 dBm output power @Channel 37 (2480 MHz)	On	On	5.69 mA
BLE_On_Transmit, 3 dBm output power @Channel 39 (2480 MHz)	On	On	4.65 mA

Note:

1. Sleep clock derived from external 32.768 kHz crystal specified for CL = 7 pF, using the default on-chip capacitance only, without using external capacitance.
2. Measurement conditions:
   2.1. VBAT=3.3V
   2.2. VDDIO=3.3V
   2.3. Temperature=25°C
   2.4. These measurements are taken with FW BluSDK Smart V6.1.6991

Figure 17-1. Average Advertising Current



Note:

1. The Average advertising current is measured at VBAT = 3.3 V, VDDIO = 3.3 V, TX output power = 0 dBm. Temperature - 25°C.
2. Advertisement data payload size - 31 octets.
3. Advertising event type - Connectable Undirected.
4. Advertising channels used in 2 channel : 37 and 38.
5. Advertising channels used in 1 channel: 37.

17.7 ADC Characteristics

Table 17-7. Static Performance of SAR ADC

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0		VBAT	V
Resolution			11		bits
Sample rate			100	1000	KSPS
Input offset	Internal VREF	-10		+10	mV
Gain error	Internal VREF	-4		+4	%

Parameter	Condition	Min.	Typ.	Max.	Unit
DNL[2]	100 KSPS. Internal VREF=1.6V. Same result for external VREF.	-0.75		+1.75	LSB
INL[2]	100 KSPS. Internal VREF=1.6V. Same result for external VREF.	-2		+2.5	LSB
THD	1 kHz sine input at 100 KSPS		73		dB
SINAD	1 kHz sine input at 100 KSPS		62.5		dB
SFDR	1 kHz sine input at 100 KSPS		73.7		dB
Conversion time			13		cycles
Current consumption	Using external VREF, at 100 KSPS		13.5		µA
	Using internal VREF, at 100 KSPS		25.0		µA
	Using external VREF, at 1 MSPS		94		µA
	Using internal VREF, at 1MSPS		150		µA
	Using internal VREF, during VBAT monitoring		100		µA
	Using internal VREF, during temperature monitoring		50		µA
Internal reference voltage	Mean value using VBAT = 2.5V		1.026 [1]		V
	Standard deviation across parts		10.5		mV
VBAT Sensor Accuracy	Without calibration	-55		+55	mV
	With offset and gain calibration	-17		+17	mV
Temperature Sensor Accuracy	Without calibration	-9		+9	ºC
	With offset calibration	-4		+4	ºC

Note:

1. Effective VREF is 2xInternal Reference Voltage.
2. These values are characterized for 0x4000F404<28:29>: 0x03 and with Vin in the range 0.25 VBAT to 0.75 VBAT. If Vin is to be used beyond this range, configure 0x4000F404<28:29> with value = 0x00.

17.8 ADC Typical Characteristics

T_C = 25ºC and V_{BAT} = 3.0V, unless otherwise noted.

Figure 17-2. INL of SAR ADC

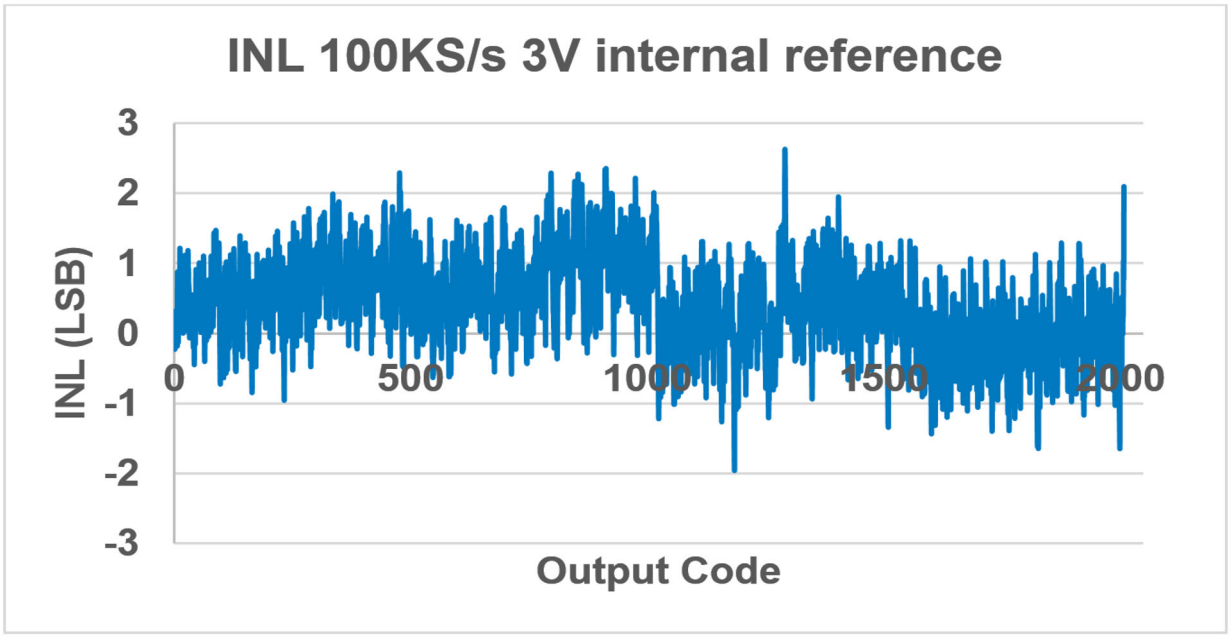


Figure 17-3. DNL of SAR ADC

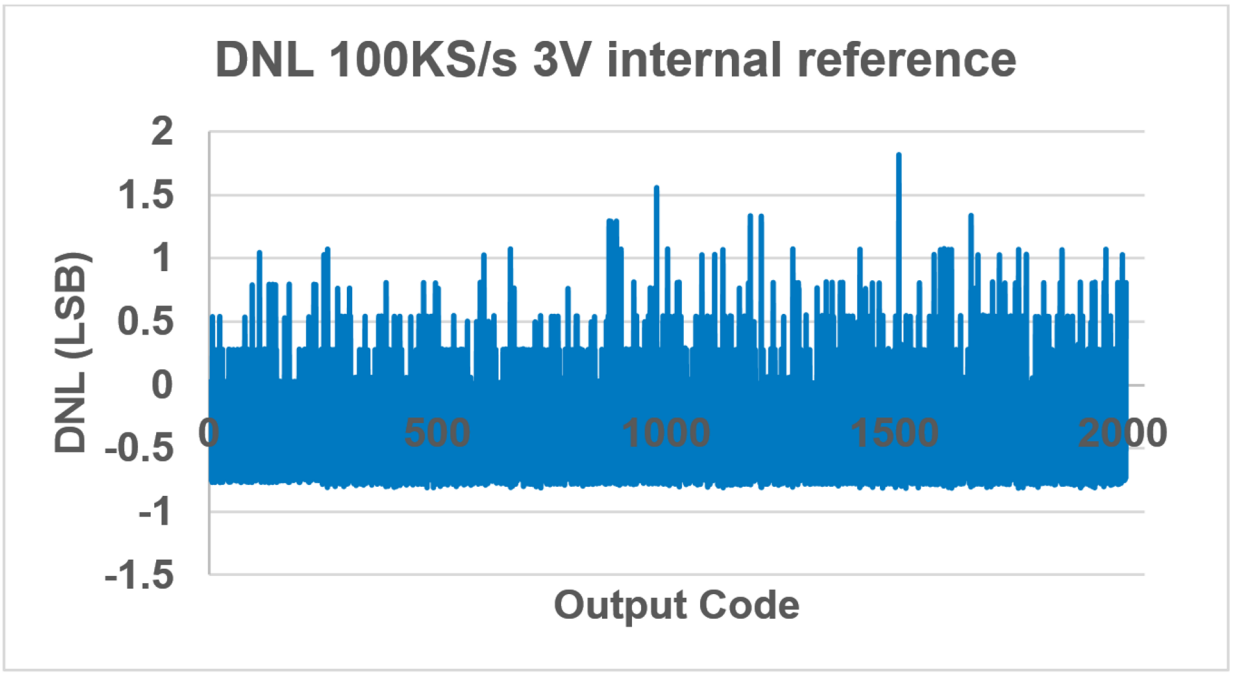
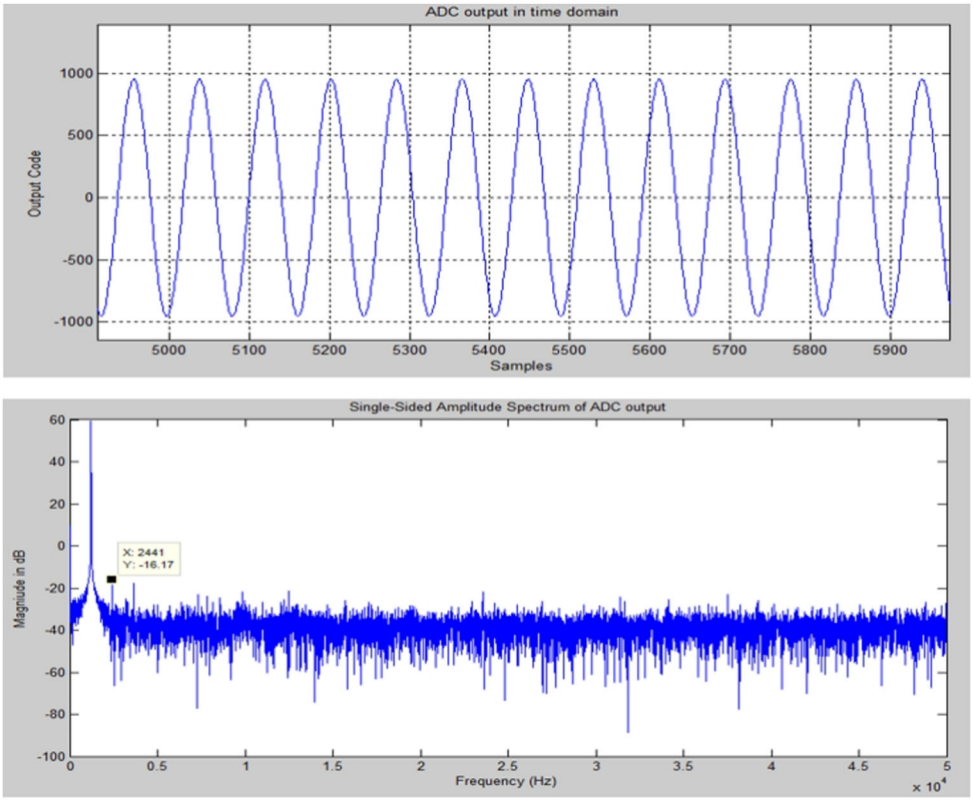


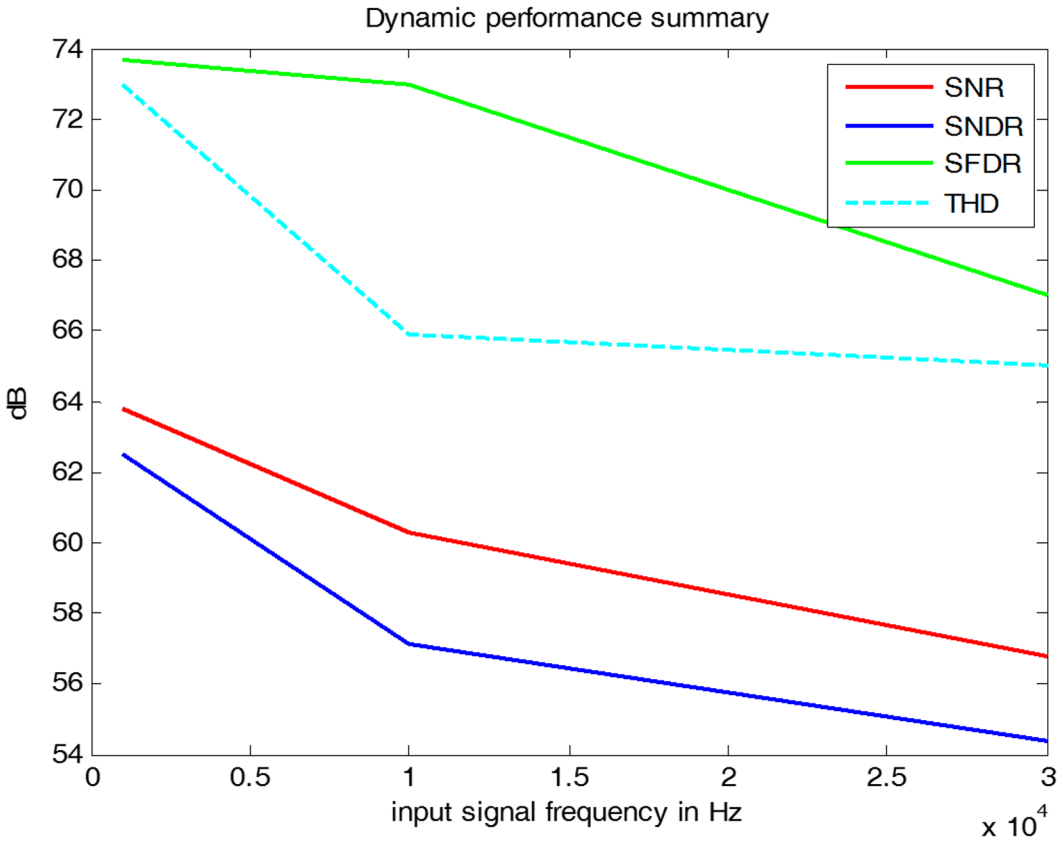
Figure 17-4. Sensor ADC Dynamic Measurement with Sinusoidal Input



Note:

1. 25ºC, 3.6V VBAT, and 100 kS/s
   . Input signal: 1 kHz sine wave, 3Vp-p amplitude.
2. SNDR = 62.5 dB
   , SFDR = 73.7 dB, and
   THD = 73.0 dB.

Figure 17-5. Sensor ADC Dynamic Performance Summary at 100 KSPS



17.9 Timing Characteristics

17.9.1 I²C Interface Timing

The I²C Interface timing (common to both Slave and Master) is provided in Figure 17-6. The timing parameters for Slave and Master modes are specified in tables Table 17-8 and Table 17-9 respectively.

Figure 17-6. I²C Slave Timing Diagram

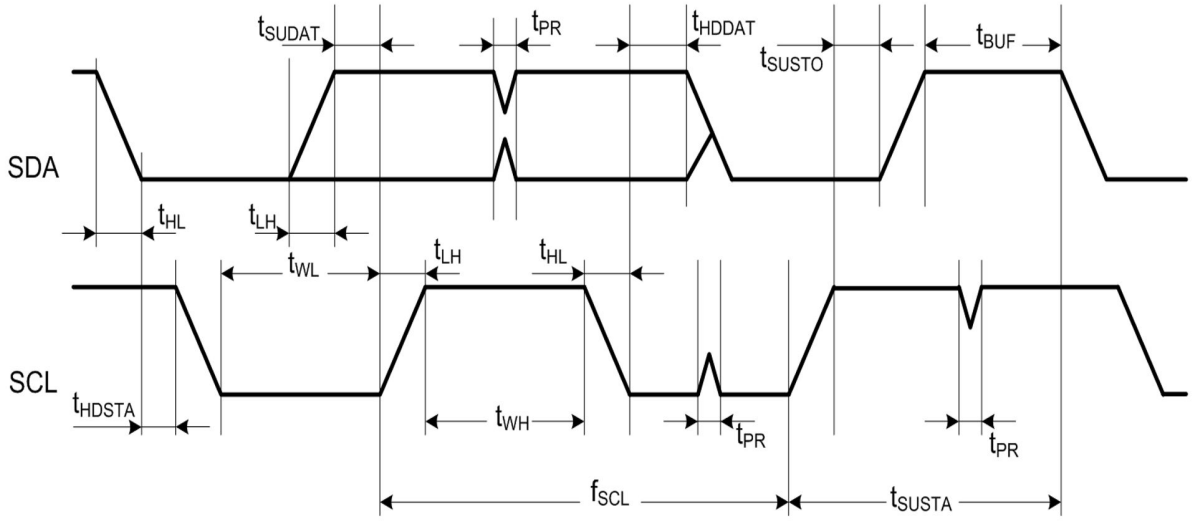


Table 17-8. I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

Table 17-9. I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

17.9.2 SPI Slave Timing

The SPI Slave timing is provided in the following figure and tables.

Figure 17-7. SPI Slave Timing Diagram

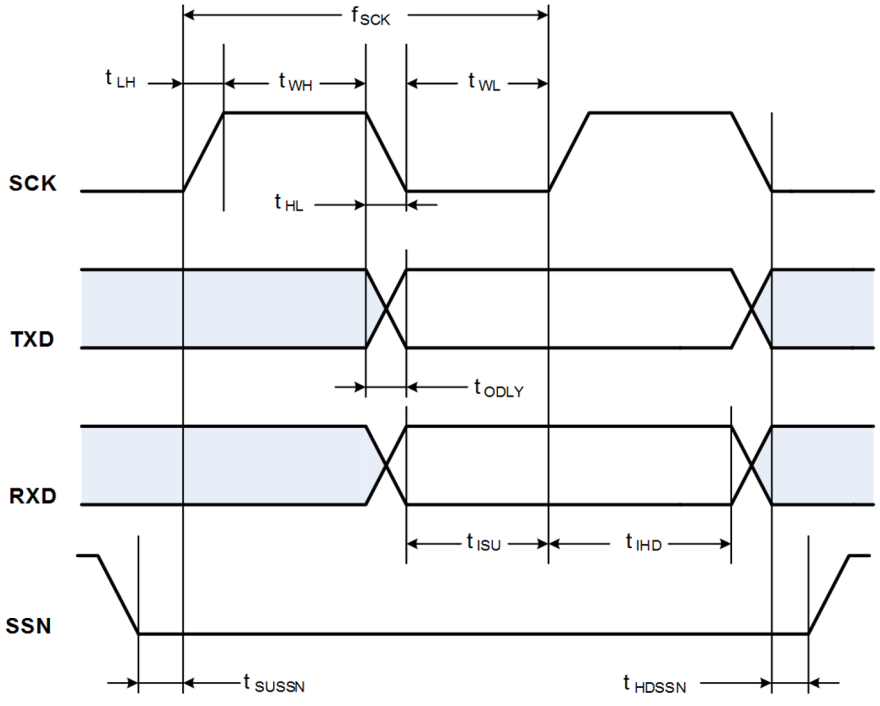


Table 17-10. SPI Slave Timing Parameters [1]

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency [2]	f_{SCK}		2	MHz
Clock Low Pulse Width	t_{WL}	55		ns
Clock High Pulse Width	t_{WH}	55		
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay[3]	t_{ODLY}	7	28	
RXD Input Setup Time	t_{ISU}	5		
RXD Input Hold Time	t_{IHD}	10		
SSN Input Setup Time	t_{SUSSN}	5		
SSN Input Hold Time	t_{HDSSN}	10		

Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design. Actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading.

17.9.3 SPI Master Timing

The SPI Master Timing is provided in the following figure and table.

Figure 17-8. SPI Master Timing Diagram

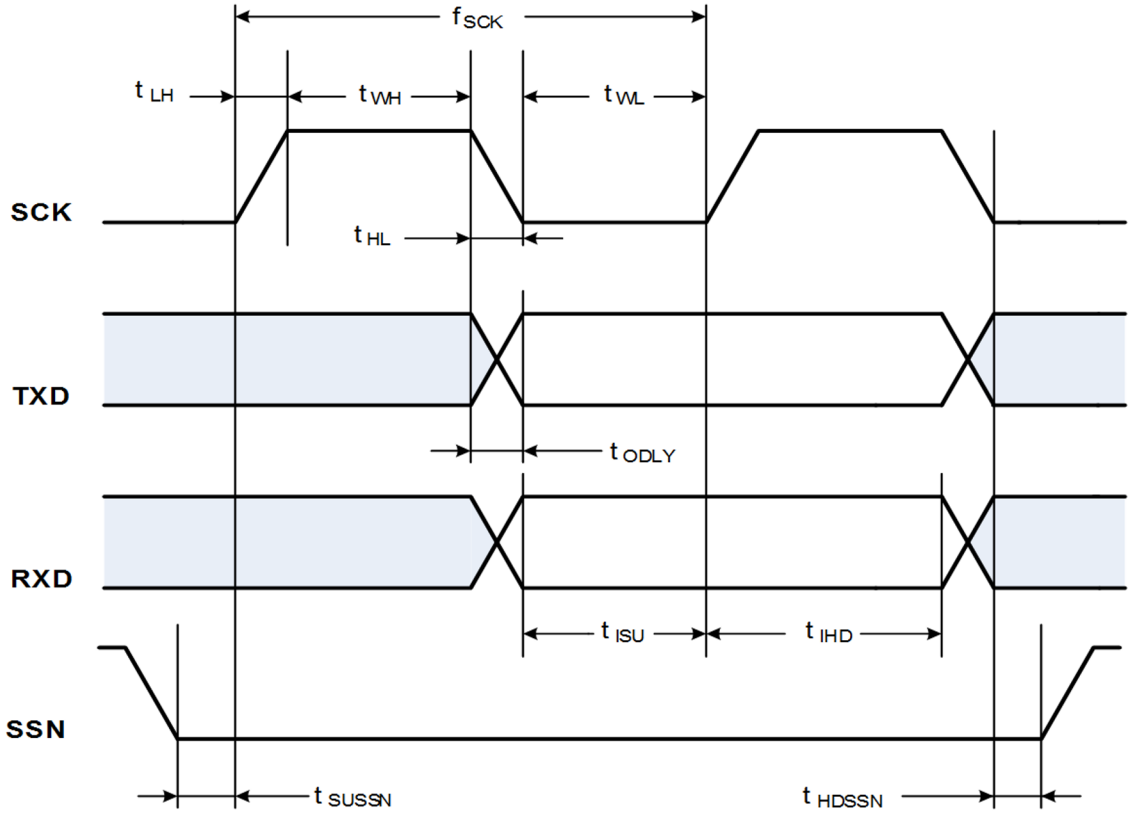


Table 17-11. SPI Master Timing Parameters(1)

Parameter	Symbol	Min.	Units	Max.
Clock Output Frequency(2)	f_{SCK}		4	MHz
Clock Low Pulse Width	t_{WL}	30		ns
Clock High Pulse Width	t_{WH}	32		
Clock Rise Time(3)	t_{LH}		7	
Clock Fall Time(3)	t_{HL}		7	
RXD Input Setup Time	t_{ISU}	23		
RXD Input Hold Time	t_{IHD}	0		
SSN/TXD Output Delay(3)	t_{ODLY}	0	12	

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Master interface internal design. The actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

17.9.4 SPI Flash Master Timing

The SPI Master Timing is provided in the following figure and table.

Figure 17-9. SPI Flash Master Timing Diagram

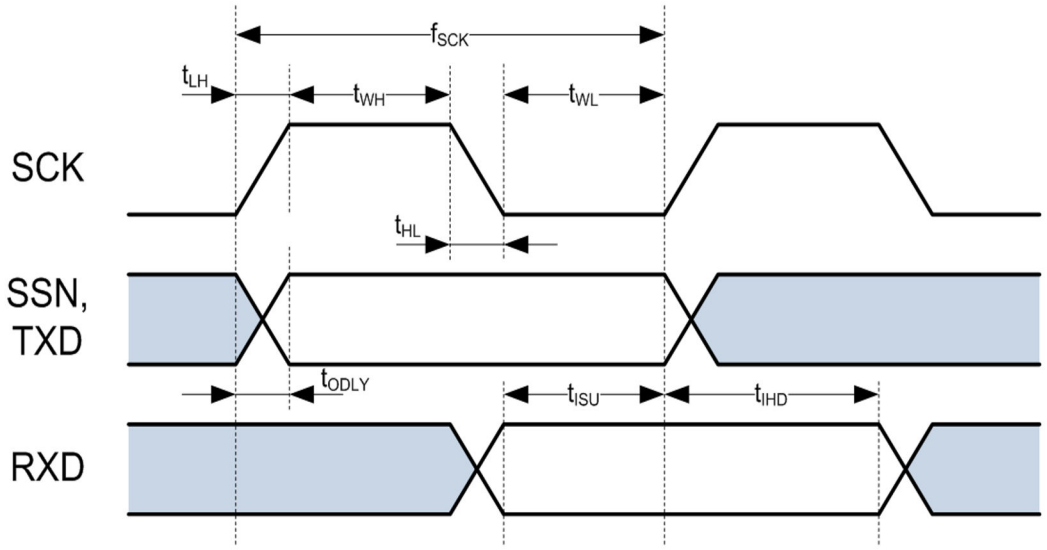


Table 17-12. SPI Flash Master Timing Parameters(1)

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency(2)	f_{SCK}		13	MHz
Clock Low Pulse Width	t_{WL}	25		ns
Clock High Pulse Width	t_{WH}	27		
Clock Rise Time(3)	t_{LH}		11	
Clock Fall Time(3)	t_{HL}		10	
RXD Input Setup Time	t_{ISU}	19		
RXD Input Hold Time	t_{IHD}	0		
SSN/TXD Output Delay(3)	t_{ODLY}	1	7	

Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Master interface internal design. Actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15 pF output loading.

18. Package Outline Drawings

18.1 Package Outline Drawing

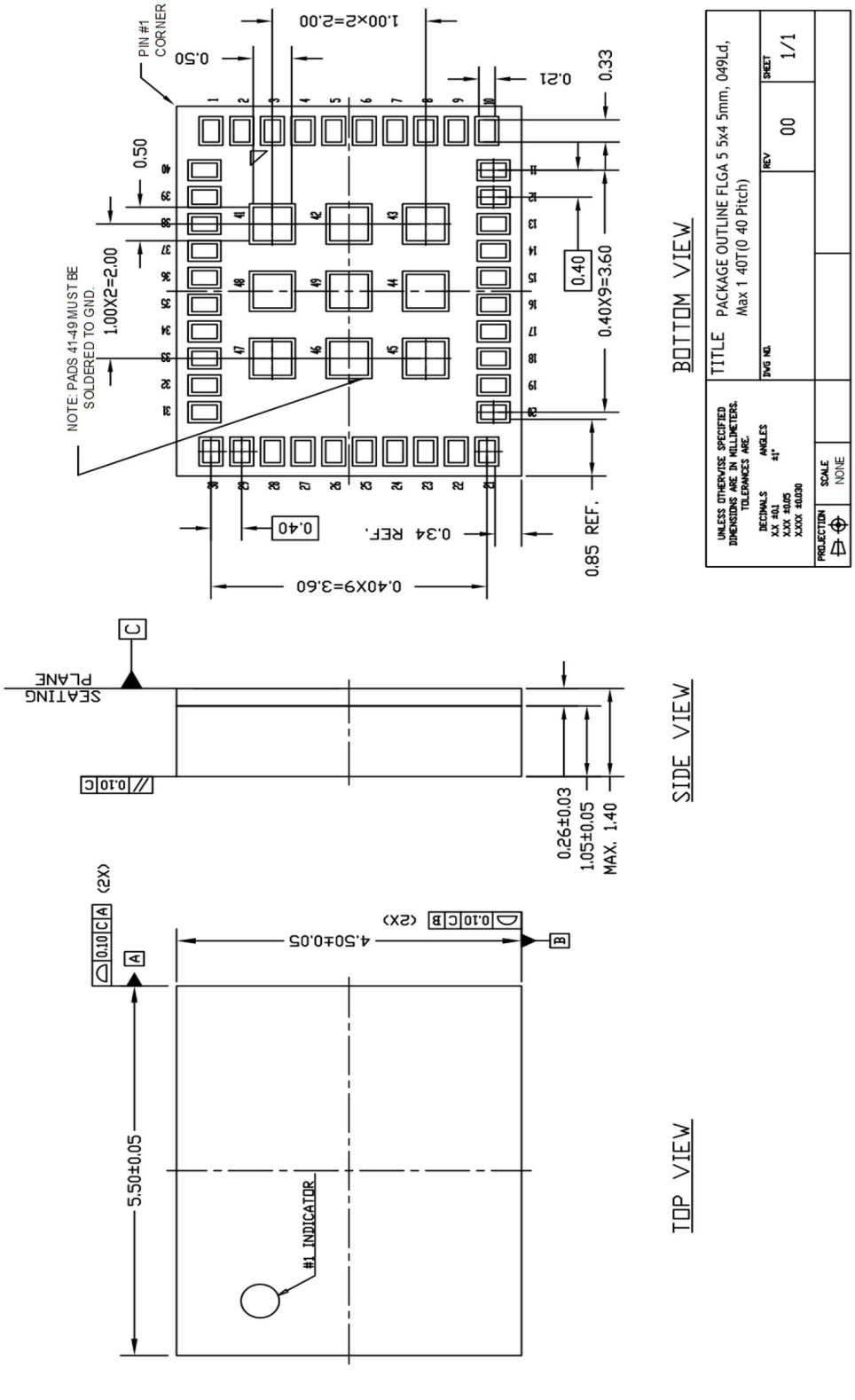
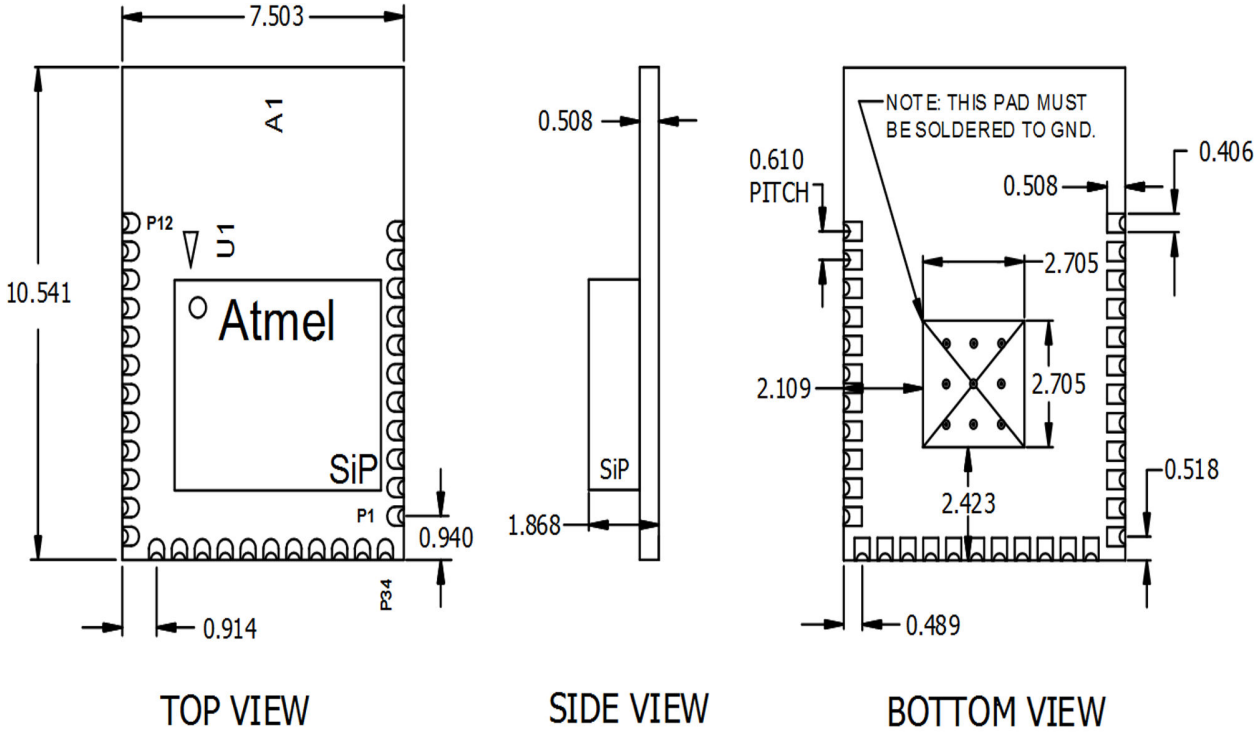


Figure 18-1. ATSAMB11-XR2100A Package Outline Drawing

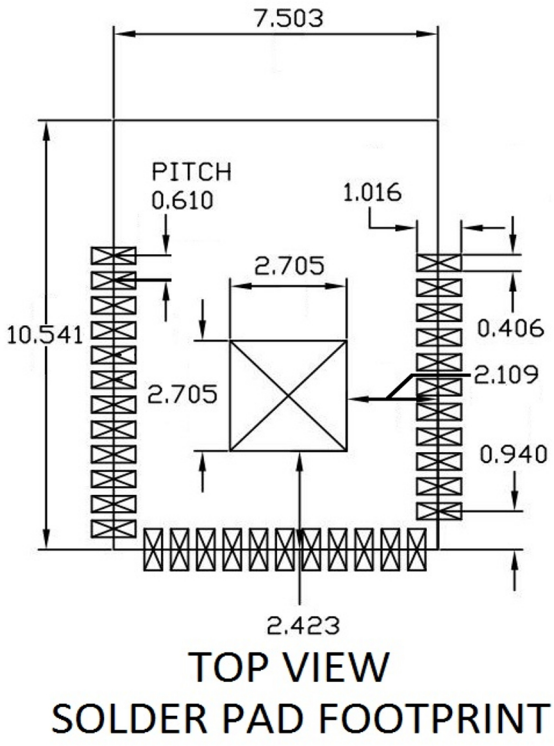
18.2 Module PCB Package Outline Drawing

Figure 18-2. ATSAMB11-ZR210CA Module Package Outline Drawing



ATSAMB11-ZR210CA
Dimension units: mm
Untoleranced dimensions
Drawing not to scale

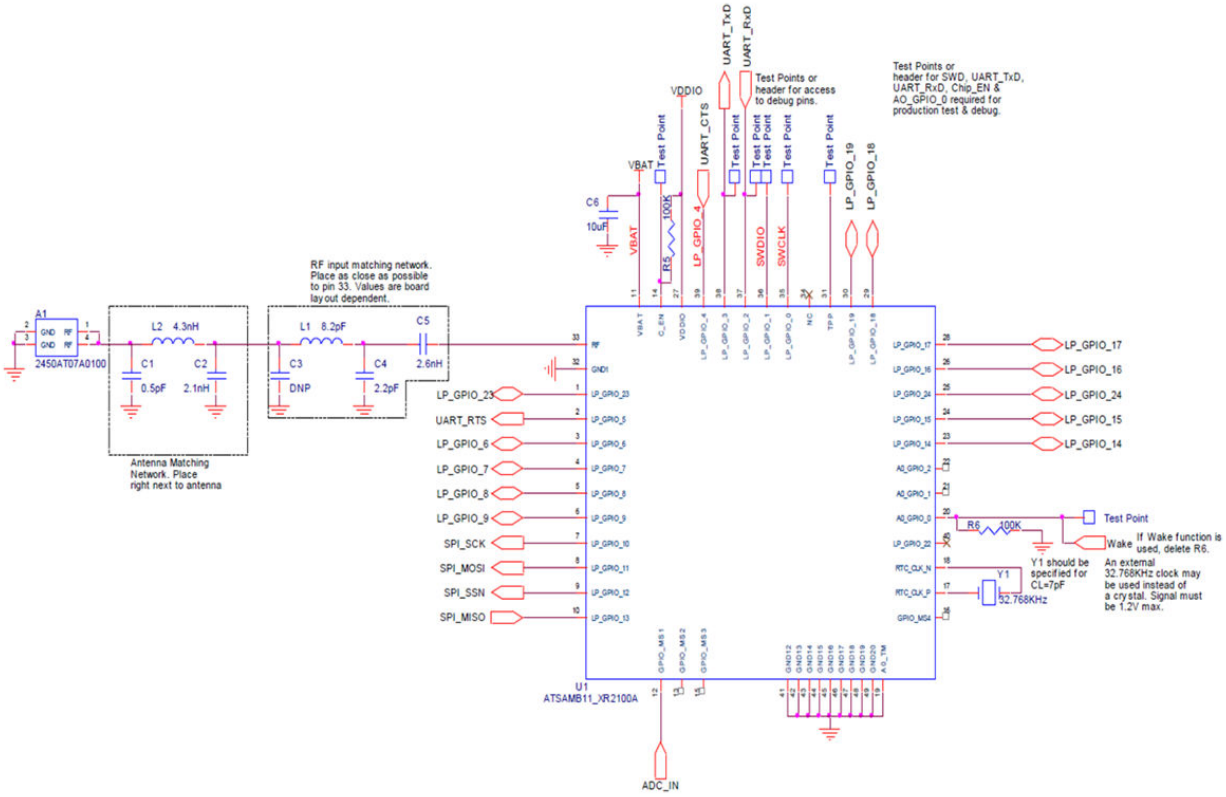
Figure 18-3. Customer PCB Top View Footprint



19. Module Reference Schematics

19.1 Reference Schematic

Figure 19-1. ATSAMB11-XR2100A Reference Schematic



19.2 Reference Schematic Bill of Materials (BOM)

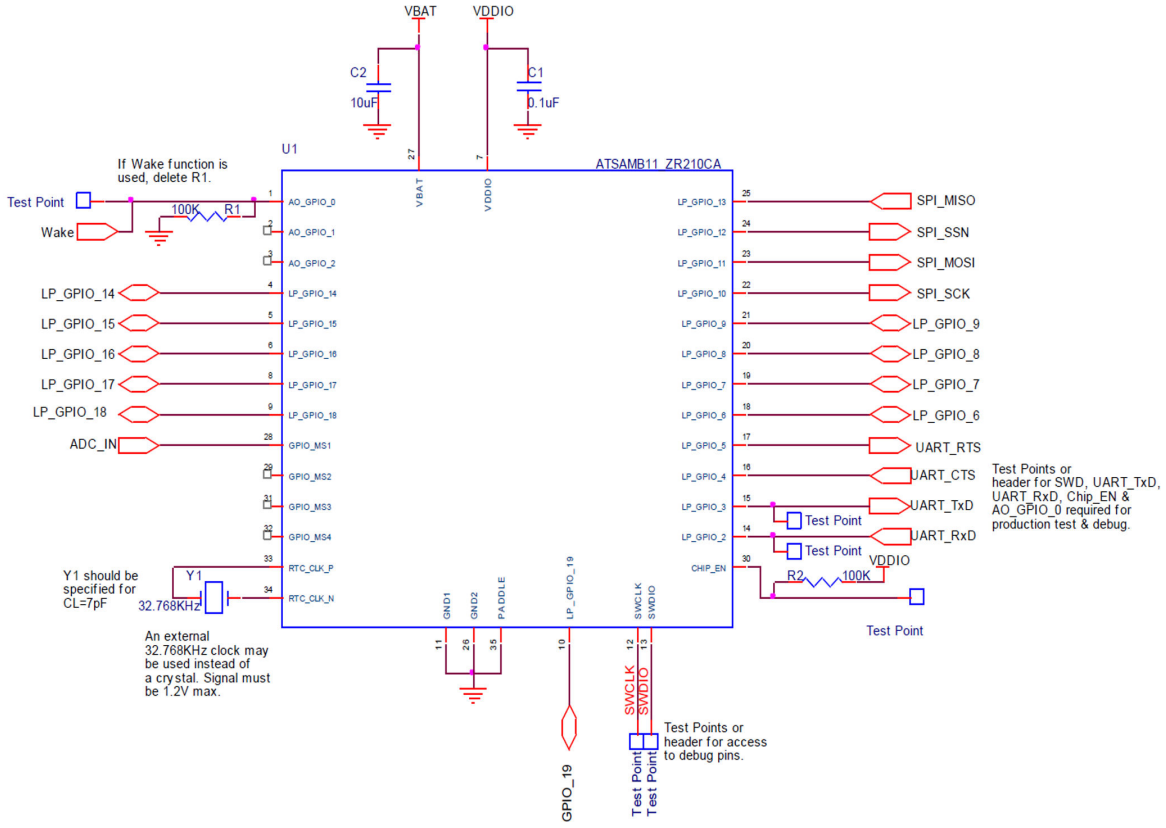
Table 19-1. ATSAMB11-XR2100A Reference Schematic Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	A1	2450AT07A0100	1x0.5 mm Ceramic Chip Antenna	Johanson Dielectrics	2450AT07A0100	
2	1	C1	0.5 pF	CAP, CER, 0.5 pF, +/-0.1 pF, NPO, 0201, 25V, -55-125 C	Johanson Dielectrics	250R05L0R5BV4T	0201
3	1	C2	2.1 nH	Inductor,2.1 nH, +/-0.1 nH, Q=14@500 MHz,	Murata Americas	LQP03TN2N1B02D	0201

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
				SRF=11 GHz, 0201, -55-125 C			
4	1	C3	DNP	CAP, CER, 2.2 pF, +/-0.1 pF, NPO, 0201, 25V, -55-125C	Johanson Dielectrics	250R05L2R2BV4T	0201
5	1	C4	2.2 pF	CAP, CER, 2.2 pF, +/-0.1 pF, NPO, 0201, 25V, -55-125 C	Johanson Dielectrics	250R05L2R2BV4T	0201
6	1	C5	2.6 nH	Inductor, 2.6 nH, +/-0.1 nH, Q=13@500 MHz, SRF=6 GHz, 0201,-55-125 C	Murata Americas	LQP03TG2N6B02D	0201
7	1	C6	10 uF	CAP, CER, 10 uF, 20%, X5R, 0603, 6.3V	AVX Corporation	06036D106MAT2A	0603
8	1	L1	8.2 pF	CAP, CER, 8.2 pF, +/-0.1 pF, NPO, 0201, 25V, -55-125 C	Johanson Dielectrics	250R05L8R2BV4T	0201
9	1	L2	4.3 nH	Inductor, 4.3 nH, +/-3%, Q=13@500 MHz, SRF=6 GHz, 0201, -55-125 C	Murata Americas	LQP03TG4N3H02D	0201
10	2	R5,R6	100K	RESISTOR, Thick Film, 100 kOhm, 0201	Panasonic®	ERJ-1GEF1003C	0201
11	7	TP1,TP2, TP4,TP5, TP6,TP7, TP8	Non-Component	Test Point,Surface Mount, 0.040"sq w/0.25"hole		40X40_SM_TEST_POINT	0.04"SQx 0.025"H
12	1	U1	ATSAMB11-XR2100A	ATSAMB11-XR2100A BLE SIP	Microchip Technology Inc	ATSAMB11-XR2100A	ATSAMB11-XR2100A
13	1	Y1	32.768 KHz	Crystal, 32.768 KHz, +/-20 ppm, -40-+85C, CL=7 pF, 2 lead, SMD	ECS, Inc. International	ECS-.327-7-34B-TR	

19.3 Reference Schematic

Figure 19-2. ATSAMB11-ZR210CA Reference Schematic



19.4 Reference Bill of Materials(BOM)

Table 19-2. ATSAMB11-ZR210CA Reference Schematic Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	C1	0.1 uF	CAP, CER, 0.1 UF 6.3V +/-10% X5R 0201	AVX Corporation	02016D104KAT2A	0201
2	1	C2	10 uF	CAP, CER, 10 uF, 20%, X5R, 0603, 6.3V	AVX Corporation	06036D106MAT2A	0603
3	2	R1, R2	100 K	RESISTOR, Thick Film, 100 kOhm, 0201	Panasonic	ERJ-1GEF1003C	0201

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
4	1	U1	ATSAMB11-ZR210CA	ATSAMB11-ZR210CA BLE Module	Microchip Technology Inc.	ATSAMB11-ZR210CA	ATSAMB11-ZR210CA
5	1	Y1	32.768 KHz	Crystal, 32.768 KHz, +/-20 ppm, -40-+85 C, CL=7 pF, 2 lead, SMD	ECS, Inc. International	ECS-.327-7-34B-TR	

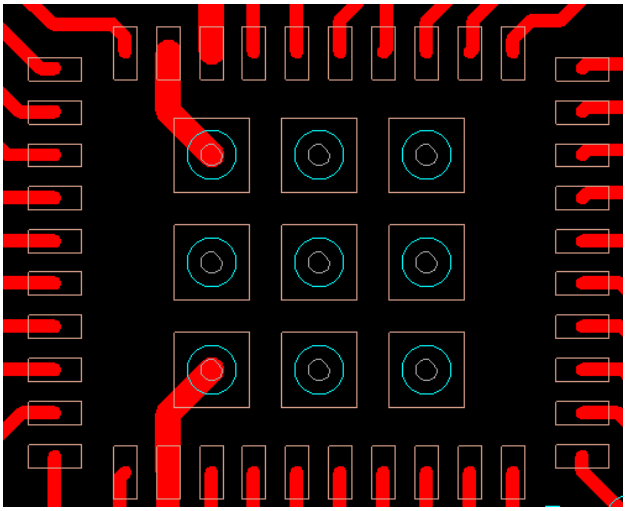
20. ATSAMB11-XR2100A Design Considerations

The ATSAMB11-XR2100A is offered in a shielded Land Grid Array (LGA) package with organic laminate substrates. The LGA package makes the second level interconnect (from package to the customer PCB) with an array of solderable surfaces. This may consist of a layout similar to a BGA with no solder spheres. However, it may also have an arbitrary arrangement of solderable surfaces that typically includes large planes for grounding or thermal dissipation, smaller lands for signals or shielding grounds, and in some cases, mechanical reinforcement features for mechanical durability.

20.1 Layout Recommendation

Referring to the SiP footprint dimensions in Figure 18-1, it is recommended to use solder mask defined with PCB pads 0.22 mm wide that have a 0.4 mm pitch. A Sample PCB pad layout in following figure shows the required vias for the center ground paddle.

Figure 20-1. PCB Footprint For ATSAMB11-XR2100A



The land design on the customer PCB should follow the following rules:

1. The solderable area on the customer PCB should match the nominal solderable area on the LGA package 1:1.
2. The solderable area should be finished with organic surface protectant (OSP), NiAu, or a solder cladding.
3. The decision on whether to have a solder mask defined (SMD) land or a non-solder mask defined (NSMD) land depends on the application space.
   - SMD: If field reliability is at risk due to impact failures such as dropping a hand-held portable application, then the SMD land is recommended to optimize mechanical durability.
   - NSMD: If field reliability is at risk due to a solder fatigue failure (temperature cycle related open circuits), then the NSMD land is recommended to maximize solder joint life.

20.1.1 Power and Ground

Proper grounding is essential for correct operation of the SiP and peak performance. Figure 18-1 shows the bottom view of the ATSAMB11-XR2100A SiP with exposed ground pads. The SiP exposed ground pads must be soldered to customer PCB ground plane. A solid inner layer ground plane should be provided. The center ground paddle of the SiP must have a grid of ground vias solidly connecting the pad to the inner layer ground plane (one via per exposed center ground pads J41 to J49).

Dedicate one layer as a ground plane, preferably the second layer from the top. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to ensure the lowest possible inductance. The power pins of the ATSAMB11-XR2100A should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have its own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

20.1.2 Antenna

When designing the ATSAMB11-XR2100A, it is important to pay attention to the following recommendations for antenna placement:

1. Make sure to choose an antenna that covers the proper frequency band; 2.400 GHz to 2.500 GHz.
2. Assure that the antenna is designed matched to 50 Ohm input impedance.
3. Talk to the antenna vendor and make sure it is understood that the full frequency range must be covered by the antenna.
4. Be sure to follow the antenna vendors best practice layout recommendations, while placing the antenna in the customer PCB design.
5. The customer PCB pad that the antenna is connected to must be properly designed for 50 Ohm impedance.
6. Make sure that the trace from the RF pin on the ATSAMB11-XR2100A to the antenna matching circuitry has a 50 Ohm impedance.
7. Do not enclose the antenna within a metal shield.
8. Keep any components that may radiate noise or signals within the 2.4 GHz to 2.5 GHz frequency band far away from the antenna and RF traces or better yet, shield the noisy components. Any noise radiated from the customer PCB in this frequency band will degrade the sensitivity of the ATSAMB11-XR2100A device.

20.2 SWD Interface

For programming and/or debugging the ATSAMB11XR/ZR, the device must be connected using the Serial Wire Debug (SWD) interface. Currently, the SWD interface is supported by Microchip programmers and debuggers SAM-ICE and ATMEL-ICE.

For ATMEL-ICE, which supports Cortex Debug Connector (10-pin) interface, the signals must be connected, as shown in Figure 20-2 with details described in Table 20-1.

Figure 20-2. Cortex Debug Connector (10-pin)

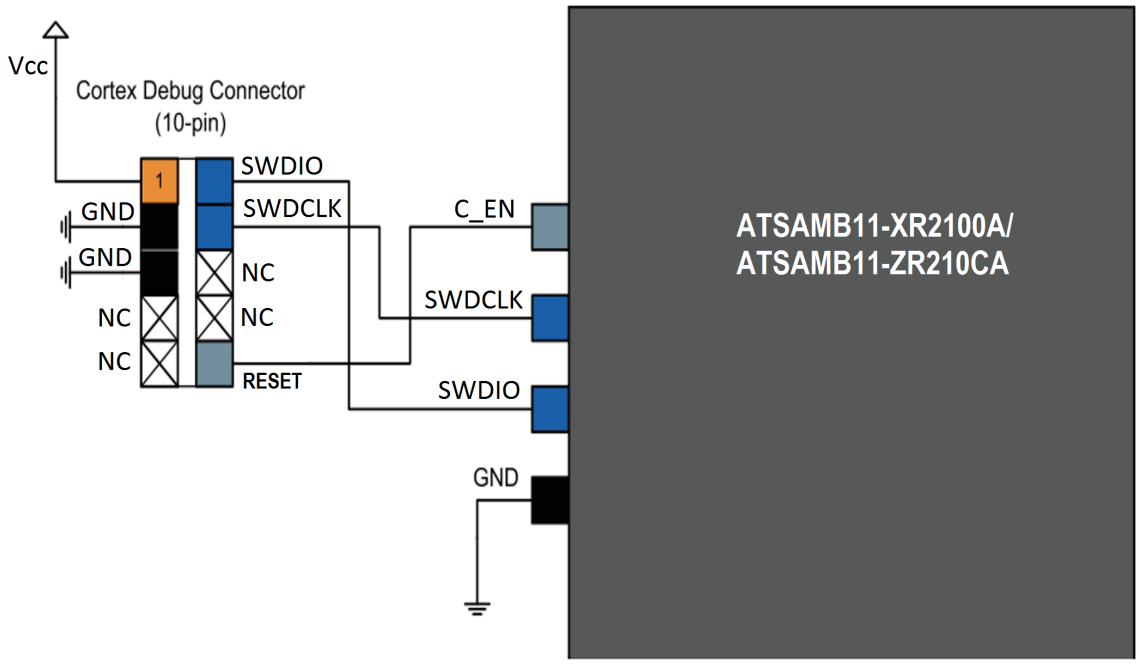


Table 20-1. Cortex Debug Connector (10-pin)

Header	Signal Name Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
C_EN	Target device reset pin, active-low
Vcc	Target voltage
GND	Ground

For SAM-ICE which support the 20-pin IDC JTAG Connector, the signals from ATSAMB11-XR2100A/ ATSAMB11-ZR210CA must be connected, as shown in Figure 20-3 with details described in Table 20-2.

Figure 20-3. 20-pin IDC JTAG Connector

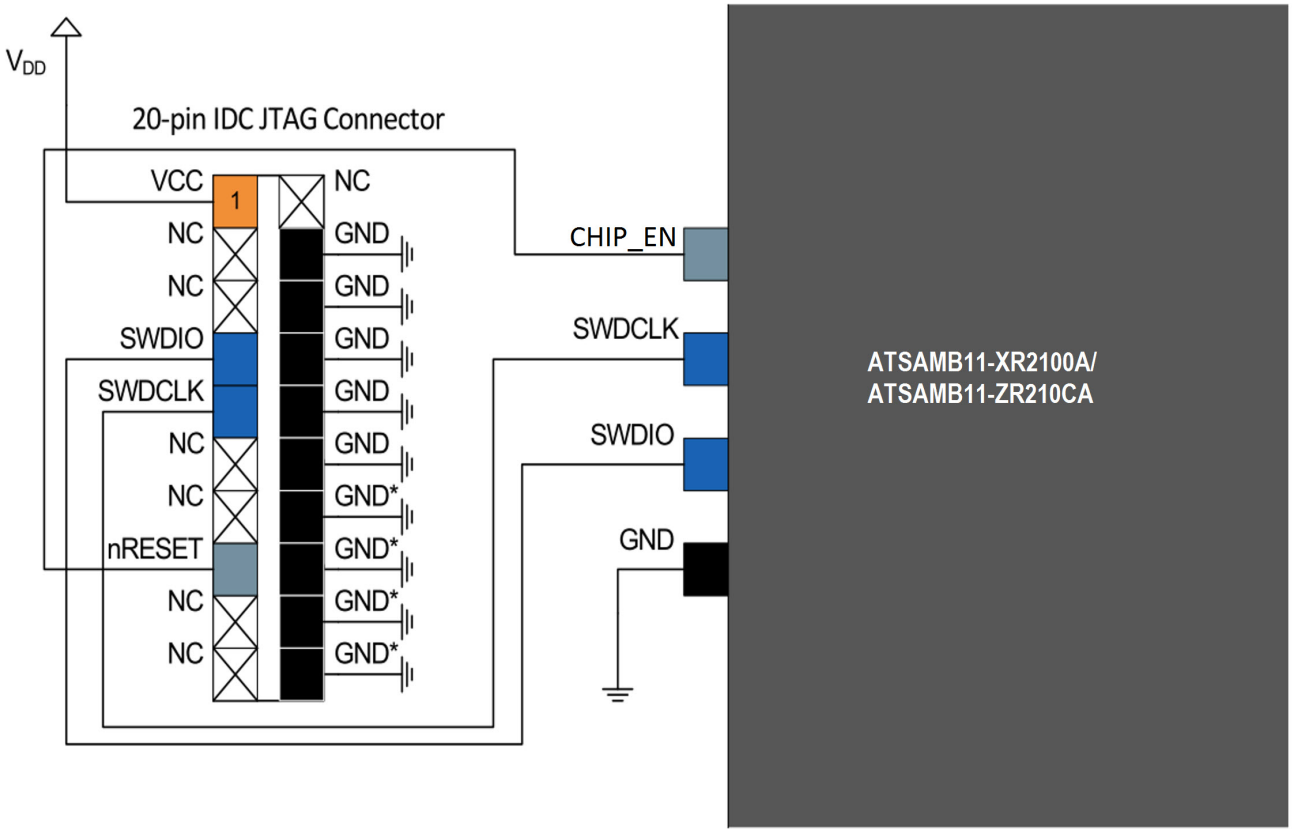


Table 20-2. 20-pin IDC JTAG Connector

Header	Signal Name Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
nRESET	Target device reset pin, active-low
Vcc	Target voltage
GND	Ground
GND*	These pins are reserved for firmware extension purposes. They can be left open or connected to GND in normal debug environment. They are not essential for SWD in general.

20.3 Unused or Unconnected Pins

Internal pull-down for unused pins must be enabled to acheive the lowest current leakage.

21. ATSAMB11-ZR210CA Design Considerations

21.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance for the ATSAMB11-ZR210CA module:

1. The host board design should have a solid ground plane. It is recommended to have a 3x3 grid of GND vias solidly connecting the exposed GND paddle of the module to the ground plane on the inner/other layers of the host board. The module ground pins should have ground vias either on or right next to the host PCB pad.
2. Place GND polygon pour below the module. Do not have any breaks in this GND plane. Place sufficient GND vias connecting this GND polygon pour with the GND plane on the inner/other layers of the host board.
3. When the ATSAMB11-ZR210CA is placed on the host board, a provision for the antenna must be made. The antenna should not be placed directly on top of the host board design as seen in the following figure (a). The best placement, for example, is placing the module at the edge of the host board such that the module edge with the antenna extends beyond the main board edge by 3 mm, as shown as (b). Alternatively, an acceptable case could be to provide a cutout in the host board, as shown as (c). The cutout should be 7.5 mm (minimum) x 3 mm as shown in the Figure 21-2.
4. Keep large metal objects as far away as possible from the antenna, to avoid electromagnetic field blocking.
5. Do not enclose the antenna within a metal shield.
6. Keep any components that may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the ATSAMB11-ZR210CA.
7. Avoid routing any traces on the top layer of the host board in the area directly below the module.

Figure 21-1. ATSAMB11-ZR210CA Placement Examples

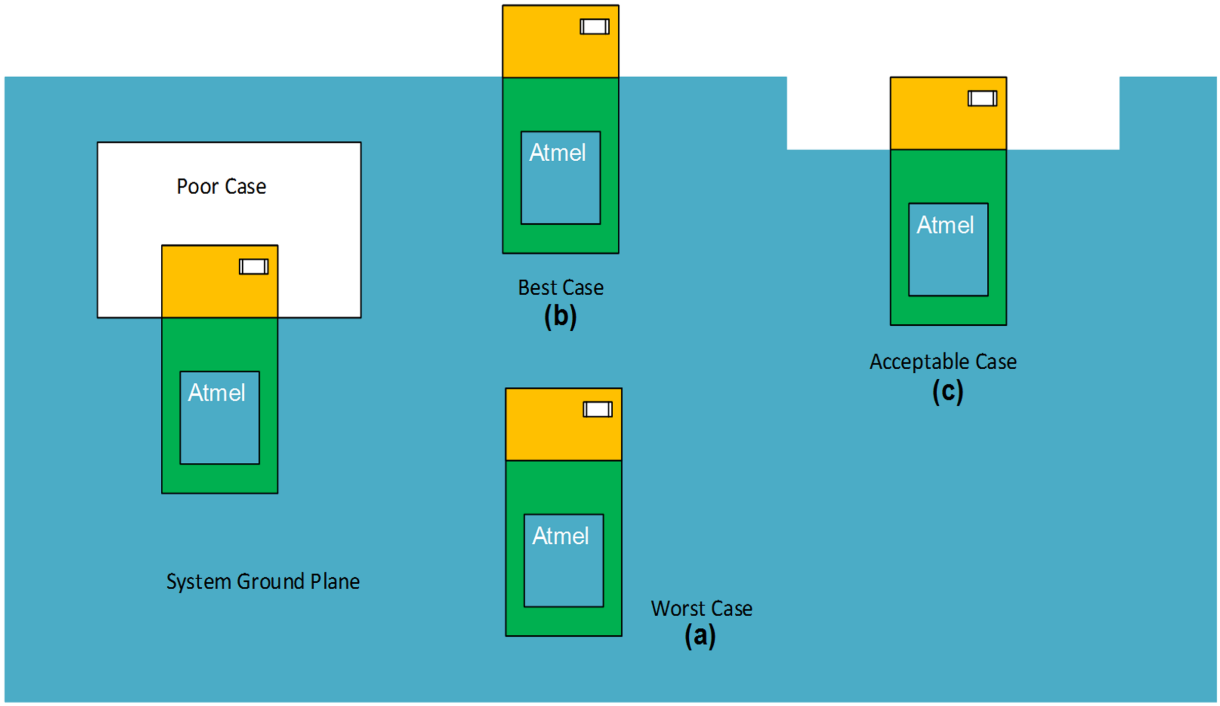
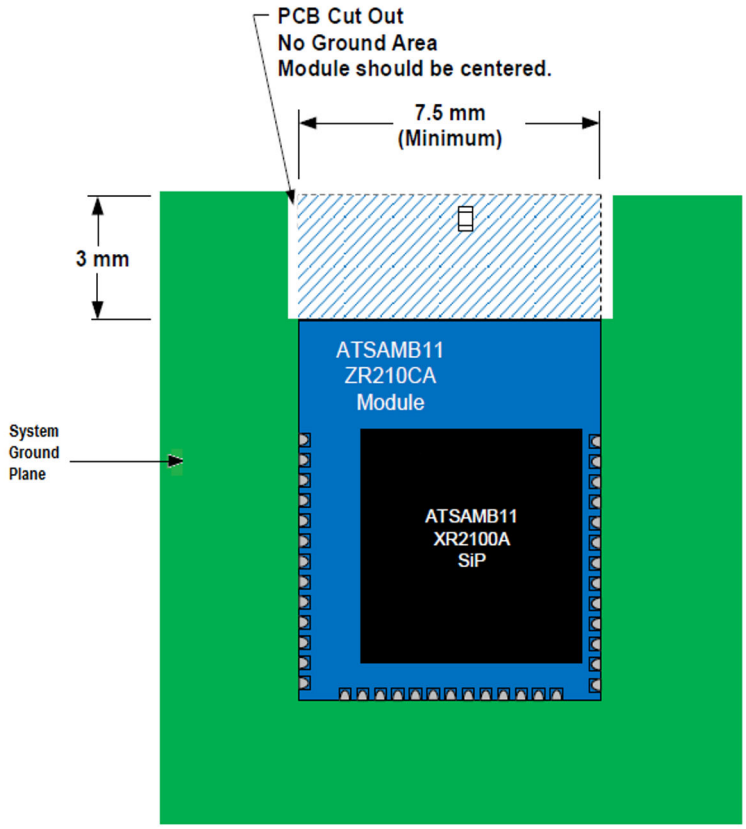


Figure 21-2. PCB Keep Out Area



21.2 Interferers

One of the biggest problems with RF devices is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there no noisy circuitry is placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

22. Reflow Profile Information

This section provides guidelines for the reflow process in soldering the ATSAMB11-XR2100A or the ATSAMB11-ZR210CA to the customer's design.

22.1 Storage Condition

22.1.1 Moisture Barrier Bag Before Opening

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

22.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

22.2 Stencil Design

The recommended stencil is a laser-cut, stainless-steel type with a thickness of 75 µm to 100 µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25 µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

22.3 Soldering and Reflow Conditions

22.3.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

Some recommended pastes include

- NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
- SENJU N705-GRN3360-K2-V Type 3, no clean paste.

Allowable reflow soldering iterations:

- Three times based on the following reflow soldering profile (see Figure 22-1).

Temperature profile:

- Reflow soldering shall be done according to the following temperature profile (see Figure 22-1).
- Peak temperature: 250°C.

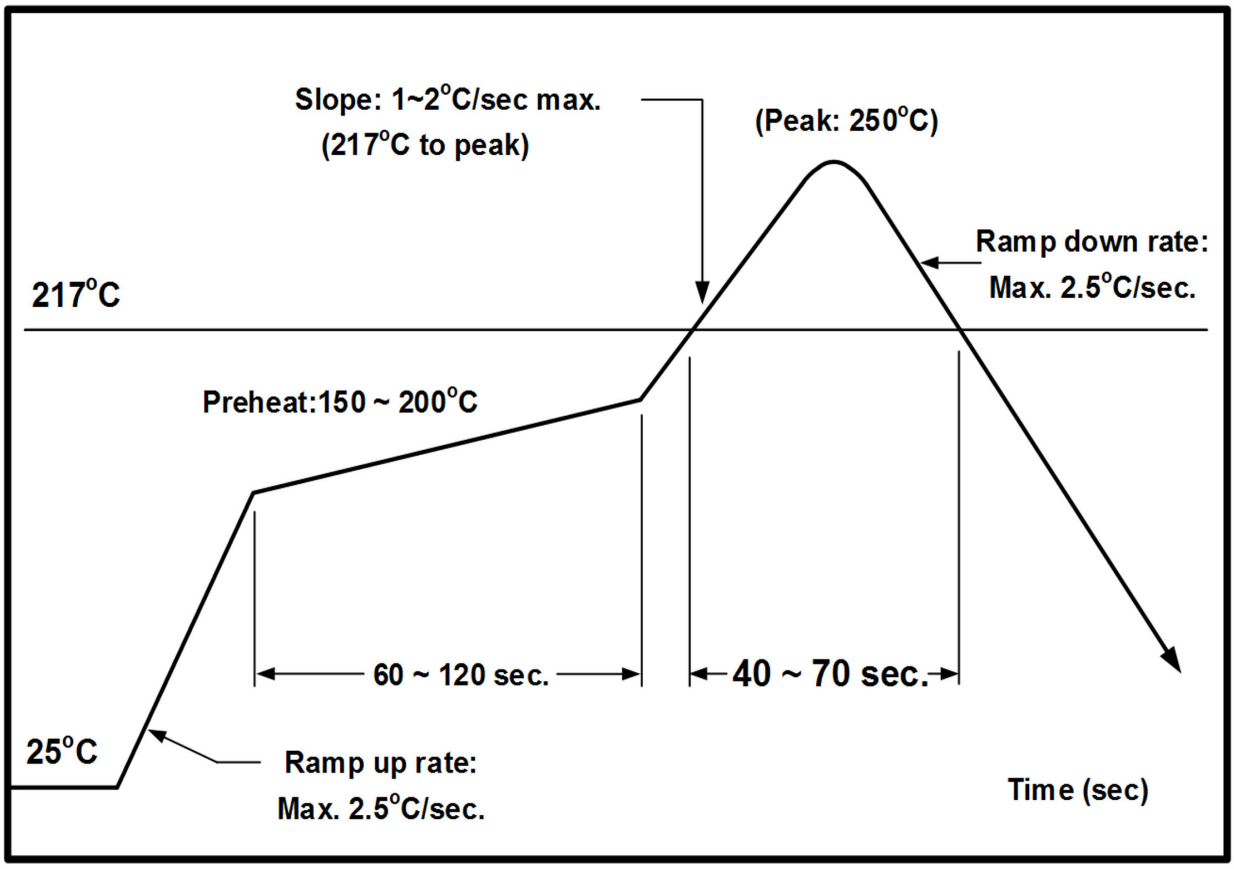
22.4 Baking Conditions

This module is rated at MSL level 3. After sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30°C/60% RH or stored at <10% RH.

The module will require baking before mounting if:

- The sealed bag has been open for > 168 hours.
- Humidity Indicator Card reads >10%.
- SiPs need to be baked for 8 hours at 125°C.

Figure 22-1. Solder Reflow Profile



22.5 Module Assembly Considerations

The Microchip ATSAMB11-ZR210CA module is manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and or applied to the ATSAMB11-ZR210CA module.

Solutions like IPA and similar solvents can be used to clean the ATSAMB11-ZR210CA module. However, cleaning solutions containing acid should never be used on the module.

23. Regulatory Approval

Regulatory approvals received:

ATSAMB11-ZR210CA

- United States/FCC ID: 2ADHKBZR
- Canada/ISED
  - IC: 20266-SAMB11ZR
  - HVIN: ATSAMB11-ZR210CA
- Europe - CE (RED)

23.1 United States

The ATSAMB11-ZR210CA module has received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification or Declaration of Conformity) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

23.1.1 Labeling And User Information Requirements

Due to the limited module size of ATSAMB11-ZR210CA (7.503 mm x10.541 mm), FCC identifier is displayed only in the datasheet and packaging box label. FCC identifier cannot be displayed on the module label. When the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

For the ATSAMB11-ZR210CA:

Contains Transmitter Module FCC ID: 2ADHKBZR

or

Contains FCC ID: 2ADHKBZR

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

A user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm

23.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power is conducted.

Module is approved for use in mixed mobile-device and portable-device exposure host platforms. The antenna(s) used with this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

23.1.3 Helpful Web Sites

Federal Communications Commission (FCC): http://www.fcc.gov

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB): https://apps.fcc.gov/oetcf/kdb/index.cfm

23.2 Canada

The ATSAMB11-ZR210CA module has been certified for use in Canada under Innovation, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

23.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 Issue 11, Section 3): The host product shall be properly labeled to identify the module within the host device.

Due to limited size of the ATSAMB11-ZR210CA (7.503 mm x10.541 mm), the Innovation, Science and Economic Development Canada certification number is not displayed on the module. Therefore, the host device must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the words “Contains”, or similar wording expressing the same meaning, as follows:

For the ATSAMB11-ZR210CA:

Contains IC: 20266-SAMB11ZR

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada’s license exempt RSS standard(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établisse-ment d'une communication satisfaisante.

23.2.2 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The device operates at an output power level which is within the ISED SAR test exemption limits at any user distance.

23.2.3 Helpful Web Sites

Innovation, Science and Economic Development Canada: http://www.ic.gc.ca/

23.3 Europe

The ATSAMB11-ZR210CA module is a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATSAMB11-ZR210CA module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2), which is summarized in Table 23-1.

The ETSI provides guidance on modular devices in the "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the testing listed in Table 23-1, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

23.3.1 Labeling and User Information Requirements

The label on the final product that contains the ATSAMB11-ZR210CA module must follow CE marking requirements.

Table 23-1. European Compliance Testing (ATSAMB11-ZR210CA)

Certification	Standards	Article	Laboratory	Report Number	Date
Safety	EN60950-1:2006/A11:2009/ A1:2010/ A12:2011/A2:2013	[3.1(a)]	TUV Rheinland, Taiwan	11062248 001	2017-08-18
Health	EN 300 328 V2.1.1/ EN 62479:2010			50098290 001	2017-09-22
EMC	EN 301 489-1 V2.1.1 EN 301 489-1 V2.2.0	[3.1(b)]		10062088 001	2017-09-22
	EN 301 489-17 V3.1.1 EN 301 489-17 V3.2.0				
Radio	EN 300 328 V2.1.1	(3.2)		50098290 001	2017-09-22

23.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in the Table 23-1 is performed using the integral chip antenna.

23.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATSAMB11-ZR210CA is in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity for this product is available at http://www.microchip.com/design-centers/wireless-connectivity/.

23.3.3 Helpful Web Sites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/. Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU): : https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_en
- European Conference of Postal and Telecommunications Administrations (CEPT): http://www.cept.org
- European Telecommunications Standards Institute (ETSI): http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA) (Previously known as R&TTE Compliance Association): http://www.redca.eu

23.4 Other Regulatory Information

- For information on the other countries jurisdictions covered, refer to the http://www.microchip.com/design-centers/wireless-connectivity
- Should other regulatory jurisdiction certification be required by the customer, or the customer need to recertify the module for other reasons, contact Microchip for the required utilities and documentation

24. Reference Documents and Support

24.1 Reference Documents

Microchip offers a set of collateral documentation to ease integration and device ramp. The following table list documents available on Microchip website or integrated into development tools.

Table 24-1. Reference Documents

Title	Content
ATSAMB11 BluSDK Smart Release Package	This package contains the software development kit and all the necessary documentation including getting started guides for interacting with different hardware devices, tools and API user manual.
BluSDK Smart BLE API Software Development Guide	This user guide details the functional description of Bluetooth Low Energy (BLE) Application Peripheral Interface (API) programming model. This also provides the example code to configure an API for Generic Access Profile (GAP), Generic Attribute (GATT) Profile, and other services using the ATSAMB11.
ATSAMB11 BluSDK SMART OTAU Profile Getting Started Guide	This document describes how to set the evaluation board for the Bluetooth Low Energy Over-the-Air Upgrade (OTAU) application supported by the ASF.
ATSAMB11 BluSDK SMART Interrupts and ULP - Architecture and Usage User's Guide	This document details the design and usage scenarios for the Atmel® ATSAMB11 peripheral interrupts and ULP feature
ATSAMB11 BluSDK SMART Example Profiles Application User Guide	This document describes how to set up the evaluation boards for various example applications supported by the Advanced Software Framework (ASF).
Ultra Low Power BLE 4.1 SiP/ Module Errata	Errata document capturing the known issues with the ATSAMB11-XR2100A SiP

For a complete listing of development support tools and documentation, visit http://www.microchip.com, or contact the nearest microchip field representative.

25. Document Revision History

Rev B - 03/2018

Section	Changes
Section 9, 10, 11, 12, 13, 14 and 15	• Added register descriptions for BLE Clock. • Updated and added register descriptions for I/O Peripheral Multiplexing and MEGAMUXing. • Added detailed information and register descriptions for various peripherals such as, muxable interrupts, GPIO pin controller, Always-On sleep timer, Pulse Width Modulation, and I^2C interface.

Rev A - 09/2017

Section	Changes
Document	• Updated from Atmel to Microchip template. • Assigned a new Microchip document number. Previous version is Atmel 42751 revision A. • ISBN number added.

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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